

DESIGN AND APPLICATION OF AN INTERMEDIATE-RELAY BASED FULL-BAY I/O SIMULATOR FOR 220 KV SUBSTATION PROTECTION AND SCADA TESTING

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Abstract - The modernization of power systems necessitates rigorous full-circuit testing prior to equipment commissioning. At 220 kV substations, these testing procedures are frequently hindered by the construction progress of primary equipment and stringent power outage schedules. This paper proposes a design solution for a full-bay equipment state simulator that relies on an intermediate-relay matrix to cover the complete hardwired binary I/Os of the investigated bay. This operating time is intentionally faster than the actual mechanical clearance time of circuit breakers (40-60 ms) while preserving the necessary inductive load characteristics. Consequently, it enables the safe validation of complex protection schemes, including Breaker Failure (50BF), Auto-Reclosing (F79), and Trip Circuit Supervision (F74). Empirical results from the Bao Loc 220 kV Substation confirm that the proposed simulator significantly expedites the testing schedule while mitigating mechanical wear risks of primary assets.

Key words - Simulator; Circuit Testing; 220 kV Substation; Control - Protection; Integrated Control

1. Introduction

In the national power transmission system, 220 kV substations play a crucial bottleneck role in distributing and connecting the power grid [1]. Ensuring the accurate operation of the control and protection system is a prerequisite, strictly stipulated in the regulations of Vietnam Electricity (EVN) and Ministry of Industry and Trade of the Socialist Republic of Vietnam [2], [3]. Full-circuit testing is the final step to confirm the correctness of the secondary design [2], [3]. However, practical implementation at 220 kV substation upgrading projects faces several major challenges: *First*, regarding operational continuity, most 220 kV substations are constructed on a rolling basis to avoid large-scale power outages; consequently, newly installed control panels cannot be connected to the primary equipment in the switchyard due to the lack of scheduled outage windows. Furthermore, there is a significant risk of equipment damage during commissioning, as functions such as breaker failure protection (50BF) and auto-reclosing (F79) require numerous switching operations of the circuit breaker. For aging circuit breakers, this continuous testing poses potential risks of mechanical and trip coil failures, violating electrical safety and periodic testing regulations [2], [3]. Finally, grid complexity exacerbates these difficulties, because the double busbar with a transfer bus configuration necessitates highly intricate interlocking circuits-such as busbar voltage selection circuits in normal operation or transfer mode via the 200 bay-that depend directly on the states of disconnectors (DS1, DS2, DS7, DS9).

To mitigate these risks and rigorously verify breaker failure logic, the IEEE C37.119-2025 standard highly recommends comprehensive functional testing [4]. Concurrently, IEEE Std 2005 provides guidelines for Hardware-in-the-Loop (HIL) simulation-based testing to safely simulate these dynamics [5].

Unlike RTDS or commercial injection test sets that utilize real-time mathematical solvers to generate continuous CT/VT fault waveforms for closed-loop transient analysis, the proposed solution has a strictly defined boundary. It focuses exclusively on covering the complete hardwired binary I/Os of the investigated bay. The hardware under test is the secondary control-protection panel, and the simulated objects are the electromechanical states and interlocking logics of the primary circuit breakers, disconnectors, and earthing switches. Therefore, this paper investigates a design solution for a full-bay equipment state simulator using an intermediate relay system. The main advantage of this simulator is its electromechanical operating time of 10-15 ms. This characteristic surpasses the actual mechanical clearance speed (40-60 ms) to prevent race conditions when verifying the 50BF logic, while maintaining the actual inductive load characteristics so that the trip circuit supervision relays do not issue false fault alarms [5], [6].

2. Theoretical basis and system modeling

2.1. Analysis of 220 kV bay control and protection architecture

The double busbar with a transfer bus system demands complex electromechanical interlocking circuits for voltage selection and transfer operation modes via the 200 bay. The execution of these functions on the Bay Control Unit (BCU) and protection relays (F21, F87L) depends absolutely on auxiliary contacts feeding back the status from the circuit breaker and disconnectors [2], [3], [7]. For SCADA testing tasks, if the primary equipment installation is incomplete, the work is interrupted. Furthermore, the trip circuit supervision relay F74 requires a continuous supervision current (I_{TCS}) flowing through the circuit breaker coil [6]. If solely using software simulation, the F74 relay will immediately issue a Trip Circuit Fault alarm.

2.2. Mathematical modeling and relay-based hardware design

The full-bay I/O simulator is designed based on a 14-magnetic-intermediate-relay matrix to fully cover the

hardwired binary inputs and outputs required by a standard 220 kV bay. Instead of random wiring, the interlocking structure of the simulator is synthesized based on Boolean algebra [8].

To accurately replicate the electromechanical behavior of the bay, the state domain for all simulated binary I/Os is defined as $\{0, 1\}$. At the 220 kV transmission level, circuit breakers operate with independent drive mechanisms for phases A, B, and C. Let $Q_{0,\theta}(t)$ be the discrete state of the CB phase $\theta \in \{A, B, C\}$ at time t . The discrete state transition equation incorporating the electromechanical self-holding mechanism and the Trip Priority logic (where a trip command unconditionally overrides a close command) at time $t + \Delta t_{sim}$ is defined as:

$$Q_{0,\theta}(t + \Delta t_{sim}) = [Cmd_{Close,\theta}(t) \cup Q_{0,\theta}(t)] \cap \neg Cmd_{Trip,\theta}(t) \quad (Eq.1)$$

For the disconnectors (Q_{DS}) and earthing switches (Q_{ES}) the permissive operating logic ensures safe mechanical interlocking. To reflect the complex double busbar configuration with a transfer bus (incorporating disconnectors DS1, DS2, DS7, DS9 and the 200 transfer bay), the generalized permissive logic governing valid disconnector switching states and busbar voltage selection (D_{sel}) is formulated as:

$$Permissive(Q_{DS}) = \neg Q_0 \cap \neg Q_{ES} \quad (Eq.2)$$

$$Permissive(DS_{sel}) = ((Q_{DS1} \cap \neg Q_{DS2}) \cup (\neg Q_{DS1} \cap Q_{DS2})) \cap \neg Q_0 \cap State(Bay_{200}) \quad (Eq.3)$$

Similarly, the earthing switch permissive condition is defined as:

$$Permissive(Q_{ES}) = \neg Q_{DS} \quad (Eq. 4)$$

Where the parameter Δt_{sim} from Eq. (1) plays a core role in the device's superiority. The selected intermediate relay matrix has an electromechanical delay time $\Delta t_{sim} \in [10, 15]$ ms. This fixed interval provides two outstanding physical advantages. First, by exceeding mechanical milestones, Δt_{sim} is significantly faster than the actual mechanical clearance time of a standard 220 kV $S F_6$ circuit breaker ($t_{CB} \approx 40 - 60$ ms) [9], which effectively prevents false race conditions that could distort the timers (t_1, t_2) during 50BF testing. Furthermore, it ensures impedance fidelity, as the intermediate relay coils possess intrinsic inductance (L) and pure resistance (R), creating an adequate equivalent impedance (Z_{sim}) for the supervision current of the F74 trip circuit supervision relay (F741, F742 phases A, B, C) to pass through without triggering fault alarms [6]. It is important to note that F74 acts strictly as a passive impedance-monitoring loop and does not actively alter the Q_0 state logic.

The integration of these mathematical and electromechanical attributes enables the simulator not only to provide comprehensive hardwired binary contacts for the BCU and Mimic panel, but also to create a precise "digital-physical replica" for the commissioning process.

2.3. Analysis of a typical 220 kV bay schematic

At 220 kV substations managed by the national power transmission, the principle schematic is a double busbar with a transfer bus; therefore, besides standard circuits at bays,

there are specific circuits such as: busbar voltage selection, operation mode selection, and transfer mode. These circuits rely on the status of disconnectors DS1, DS2, DS7, and DS9 to operate. The status of these disconnectors also plays a vital role when the substation utilizes the 200 bay as a transfer bay.

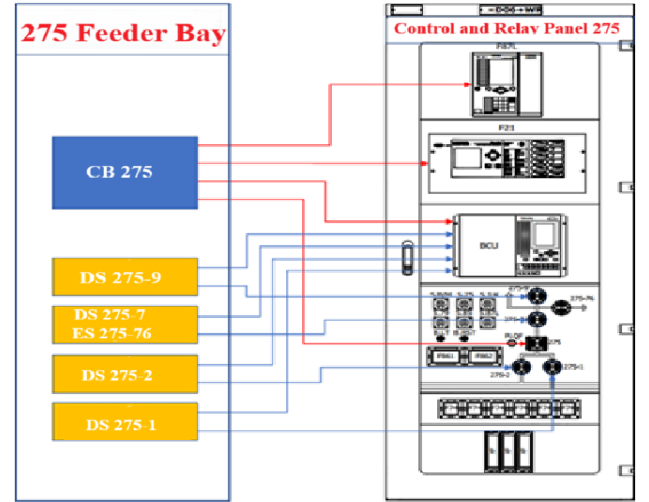


Figure 1. Signal connection model from the 275 bay equipment to the D06+WR control and protection cabinet at the Bao Loc 220 kV Substation

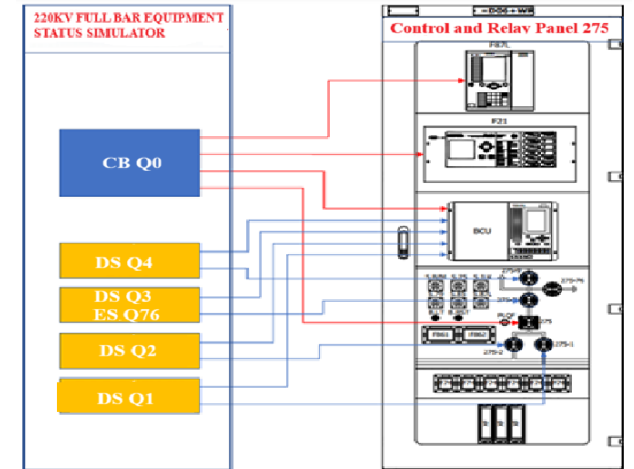


Figure 2. Signal connection model from the 220 kV bay equipment simulator to the D06+WR control and protection cabinet at the Bao Loc 220 kV Substation

To accurately replicate this schematic, the 220 kV bay equipment state simulator is composed of a 14-intermediate-relay matrix, connecting cables, and terminal jacks. The simulated components include:

(i) A circuit breaker Q_0 with multiple pairs of normally closed (52B) and normally open (52A) contacts providing 52A, 52B signals (phases A, B, C) to relays F87L, F21, serving 1-phase or 3-phase trip protection functions, auto-reclosing functions, while also providing signals to the BCU and status indicator lights on the Mimic panel. Closing/tripping commands are executed from the BCU and control switches;

(ii) Two trip coils of circuit breaker Q_0 connect to trip circuit supervision relays: F741 (A, B, C) and F742 (A, B, C) performing the trip circuit supervision function for circuit breaker 275;

(iii) Four disconnectors Q1, Q2, Q3, Q4 connect signals to the BCU and status indicator lights on the Mimic panel to simulate disconnector equipment states. Equipment opening/closing commands are executed from the BCU and control switches, connecting signals to the voltage selection circuit for protection and measurement devices;

(iv) Two earthing switches, Q75 and Q76, connect signals to the BCU and status indicator lights on the Mimic panel to simulate the state of the earthing switch equipment. Equipment opening/closing commands are executed from the BCU and control switches to the devices.

The closing/tripping coils of the circuit breaker simulator coordinate with relays F741 and F742 to perform the continuous trip circuit supervision function in both circuit breaker closed and open states. The detailed wiring connections for these devices within the control and protection cabinet are illustrated in Figures 3 to 9.

The closing/tripping coils of the circuit breaker simulator coordinate with relays F741 (A, B, C) and F742 (A, B, C) to perform the trip circuit supervision function, supervising in the following cases: (i) Circuit breaker closed (F741; F742 phases A, B, C) combined with the circuit breaker closing coil. (ii) Circuit breaker open (F741; F742 phases A, B, C) combined with the circuit breaker trip coil.

The wiring connections for the circuit breaker, disconnectors, and earthing switches within the control and protection cabinet are illustrated in Figures 6, 7, 8, and 9.

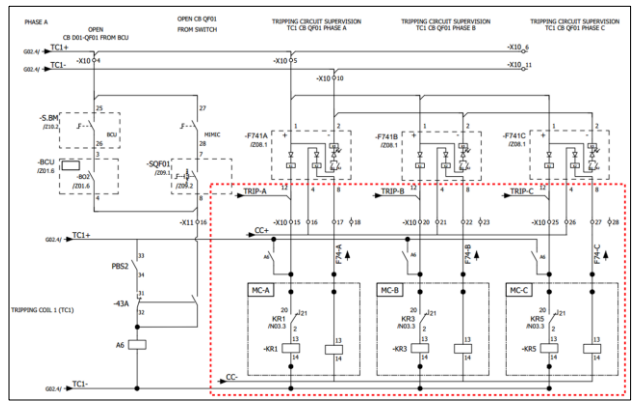


Figure 5. Circuit diagram for circuit breaker tripping commands from the Mimic control switch and BCU, incorporating F74 supervision, to the simulator

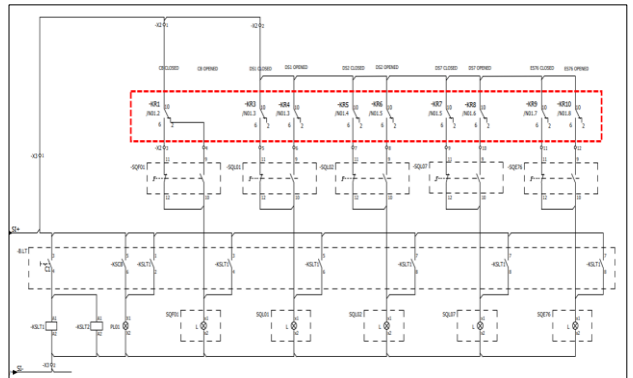


Figure 6. Connection diagram for circuit breaker, disconnector, and earthing switch status signals from the simulator to the Mimic panel

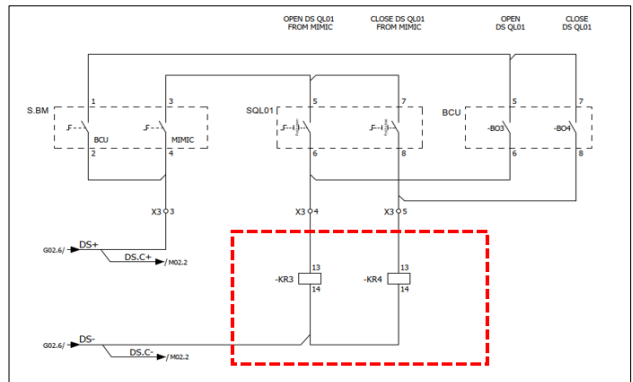


Figure 7. Circuit diagram for disconnector opening/closing commands from the Mimic control switch to the simulator

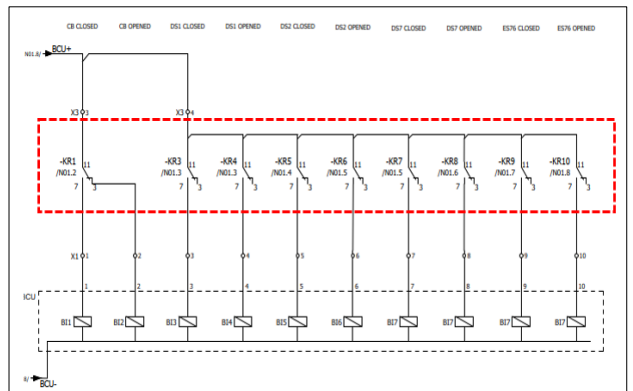


Figure 8. Wiring diagram for circuit breaker, disconnector, and earthing switch status inputs from the simulator to the BCU

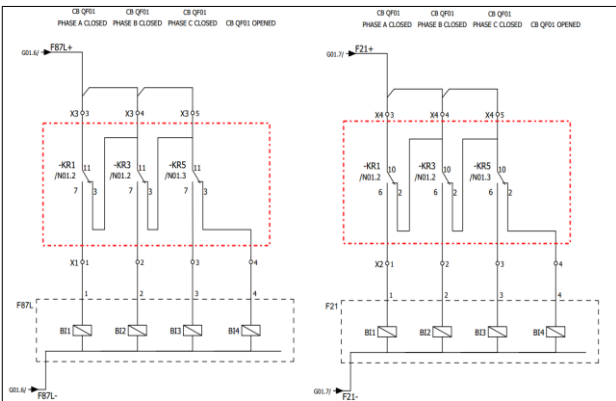


Figure 3. Connection diagram of the circuit breaker status in the simulator to the F21 and F87L relays

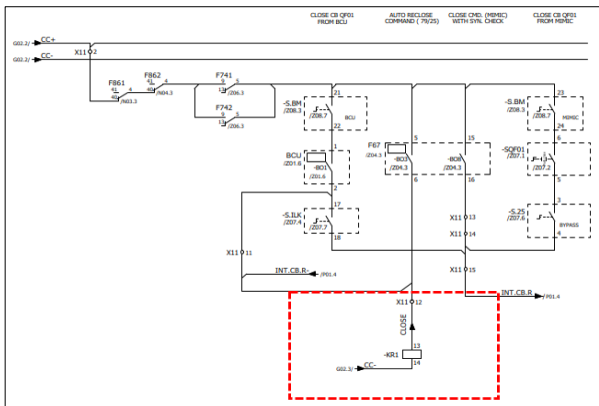


Figure 4. Circuit diagram for circuit breaker closing commands from the Mimic control switch, BCU, and F79 auto-reclosing function to the simulator

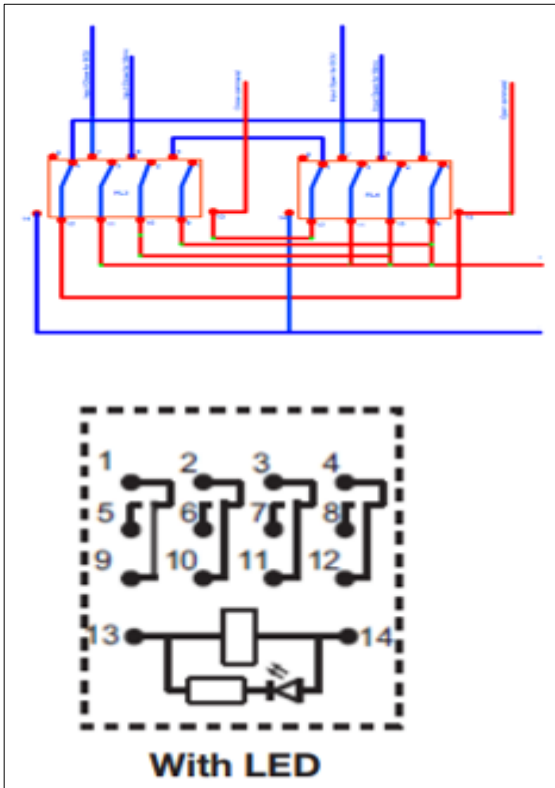


Figure 9. Detailed wiring diagram of the auxiliary contacts for each intermediate relay pair within the simulator

(Source: Adapted from manufacturer datasheet)

2.4. Requirements for the simulator

A standard 220 kV substation bay includes: (i) Circuit breaker: Independent three-phase drive, requiring individual phase status monitoring and independent trip circuit supervision; (ii) Disconnectors: Serves to connect busbar C21, C22, transfer bus or earthing switch (Q76). The secondary circuit of this bay must send status signals to the BCU for the SCADA system and simultaneously to the main protection relays (F21, F87L) to execute protection logic.

To completely replace primary equipment during testing, the simulator must meet specific requirements: *First*, provide auxiliary contacts 52A (normally open) and 52B (normally closed) corresponding to phases A, B, C of the circuit breaker. *Second*, simulate closing/tripping coils with suitable resistance so that the trip circuit supervision relays (F741, F742) do not report errors. *Third*, provide continuous status feedback to the Mimic system and station-level SCADA according to technical standards [3]. *Fourth*, possess the ability to self-hold the state after receiving control commands to accurately simulate the mechanical position of the primary equipment.

To clarify the specific scope of the proposed hardware, Table 1 presents the detailed binary I/O mapping of the simulator. The system strictly covers the hardwired binary interfaces of the investigated 220 kV bay.

Table 1. Binary I/O Mapping Table for 220 kV Bay Simulator

Primary Equipment	Simulated Status/Command	Simulator Component (Intermediate Relay)	Supported Protection/Control Logic
Circuit Breaker (Q0)	52a (NO), 52b (NC) (Phases A, B, C)	Relays KR1, KR2, KR3 (Coil and Contacts)	F21, F87L, 50BF, F79, BCU indication
	Close Command / Trip Command	KR1, KR2, KR3 Operation	BCU Control, Auto-reclose (F79)
	Trip Circuit Supervision (I_{TCS})	Equivalent inductive coil load	F741, F742
Disconnectors (Q1, Q2, Q3, Q4)	89a (NO), 89b (NC) (Open/ Closed status)	Relays KR4 to KR7	Busbar voltage selection, Interlocking
Earthing Switches (Q75, Q76)	89a (NO), 89b (NC) (Open/ Closed status)	Relays KR8, KR9	BCU Interlocking logic

(Source: Author's compilation)

2.5. Hardware Component Specifications

To validate the physical feasibility of the simulator, the electrical specifications of the selected intermediate relays (KR) and the power supply system must be clearly defined.

2.5.1. Relay Coil Impedance and F74 Compatibility

In actual substations, the Trip Circuit Supervision relay (F74)-specifically utilizing the GE MVAX12/Ediseja TCS monitoring architecture-injects a continuous measuring current (I_{TCS}) through the circuit breaker's trip circuit. To prevent the F74 from issuing false "Trip Circuit Fault" alarms, the simulator's intermediate relay (KR) coils are characterized by an assigned nominal inductance of $L \approx 1.35$ H combined with a DC coil resistance within the range of $R=54-65$ k Ω (specifically 58 k Ω in this hardware configuration). Under the station's ungrounded 220 VDC battery supply, this electromagnetic configuration establishes a steady monitoring current. The non-operating threshold of these commercial F74 relays is strictly below 1mA, whereas the simulator's sustained monitoring current was verified through a 72-hour continuous endurance test, yielding stable statistical metrics of Min = 3.41 mA, Mean = 3.45 mA, and Max=3.50 mA. Furthermore, an intentional open-circuit test was executed by breaking the monitoring loop; the F74 relay accurately detected the current drop to 0 mA, successfully exceeding its drop-out threshold and issuing an alarm output within a standard time delay of $t \approx 2.5$ s.

2.5.2. DC Power Supply Configuration

Unlike laboratory models that rely on low-voltage 12V/24V sources, the proposed simulator is engineered to operate directly from the substation's standard ungrounded battery bank. The system is rated for an operating voltage of $V_{DC}=220$ V (with an allowable tolerance of 80%-110%). The maximum power consumption of the *entire 14-relay matrix*, assuming an extreme case where all elements are energized simultaneously, is strictly bounded below

$P_{max}=15\text{ W}$. This minimal load ensures that the simulator can be safely powered by the existing secondary MCBs without imposing any thermal or electrical stress on the actual station's DC distribution board.

2.5.3. Electromechanical Timing Characteristics

To address the precise coordination required for protection relays, the switching kinematics of the KR relays were bench-tested under the nominal 220 VDC supply. The measured timing parameters are: pull-in time $t_{pull-in} \approx 5\text{-}20\text{ ms}$, drop-out time $t_{drop-out} \approx 10\text{-}20\text{ ms}$, and contact bounce time $t_{bounce} \leq 5\text{ ms}$. These inherent fixed latencies form the physical baseline for validating time-dependent protection logic such as breaker failure (50BF).

3. Experimental Results And Benchmarking

The device has been put into practical application in the control and protection system upgrade project at the Bao Loc 220kV Substation. Testing was conducted in parallel to optimize the schedule while waiting for the primary equipment installation to be completed.

3.1. System indication and control function testing

In terms of display, the status of the entire bay is accurately displayed on the BCU's LCD screen and the control-protection cabinet's Mimic panel. In terms of control, remote opening/closing commands from the Southern Regional Load Dispatch Center (A2) are immediately executed and responded to by the simulator, allowing the verification of the entire data flow from the bay-level equipment to the station level and back to the control center [10]. The physical I/O model of the simulator responds continuously, ensuring absolute reliability of operational commands without generating unintended communication delays.

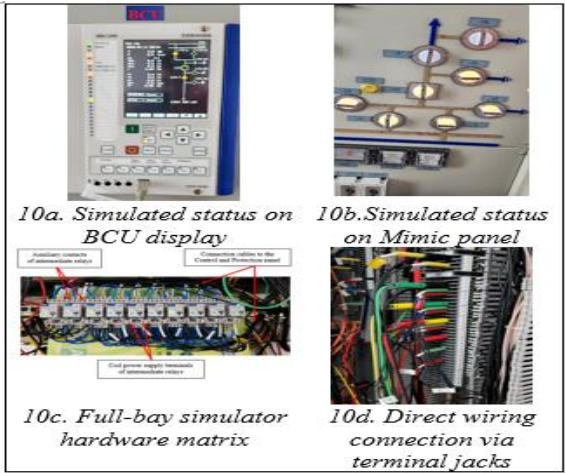


Figure 10. Field application at Bao Loc 220 kV Substation

The empirical application results at the Bao Loc 220kV Substation are illustrated in Figure 10. Specifically, the simulator's hardware matrix and its jack-based connection to the control panel are shown in Figure 10c and 10d. The continuous status feedback from the simulator is accurately acknowledged and displayed on the BCU interface (Figure 10a) and the Mimic panel (Figure 10b), demonstrating that the system has effectively resolved the equipment status simulation challenges without data latency.

To quantitatively validate the reliability and stability of the simulator, a comprehensive experimental testing matrix was executed during the commissioning phase at the Bao Loc 220 kV Substation. The measurement instruments included OMICRON CMC 356 for time-domain sequence testing and generic oscilloscopes for latency measurement. Table 2 details the standardized test cases, acceptance criteria, and measured empirical results over multiple iterations.

Table 2. Comprehensive Experimental Testing Matrix for 220 kV Bay Simulator

Test Function	Initial Condition	Actuating Signal	Pass/ Fail Criteria (Expected Result)	Iterations	Measured Latency / Response	False Alarms	Test Result
BCU/ Mimic Indication	CB and DS Open (State 0)	Close Command from BCU	Accurate state change to "Closed" (State 1)	50	10-15 ms (Local I/O)	0	Passed
SCADA End-to-End	CB Closed (State 1)	Open Command from A2 Dispatch	CB status updates on SCADA HMI $\leq 2.0\text{ s}$	30	$< 0.8\text{ s}$ (End-to-End)	0	Passed
Interlocking Logic	CB Closed Earthing Switch (ES) Open	Open Command to DS	Command strictly blocked by BCU logic	20	N/A (Blocked)	0	Passed
50BF Logic	CB Closed	Relay Trip Cmd + CB Failure (Blocked coil)	t_1, t_2 timers expire exactly at settings	20	Timer drift $\leq 2\text{ ms}$	0	Passed
F79 Auto-Reclose	CB Closed	Single-phase fault trip signal	Trip $\rightarrow$ Reclose $\rightarrow$ Maintain state exactly per deadtime	20	Mechanical race conditions eliminated	0	Passed
F74 Supervision	CB Open / CB Closed	Steady 220VDC supply	Maintain monitoring current (I_{rcs}), no fault	Continuous (72h)	Stable at 3.5 mA	0	Passed
Busbar Transfer Interlocking (DS1/DS2)	Busbar C21 selected, CB Open	Switchover command to Busbar C22 via DS1/DS2	Validates correct permissive interlocking state prior to transfer	20	10-15 ms	0	Passed
Transfer Bus (Bay 200) Interlocking	Normal operation via main bus	Transfer mode command via DS7/DS9	System blocks unsafe operations unless transfer bay conditions are met	20	N/A (Blocked)	0	Passed

(Source: Author's compilation)

To rigorously validate the complete state space coverage of the hardware control algorithm, Table 2 has been expanded to encompass comprehensive interlocking test scenarios. These include standard busbar selections (C21/C22), transfer bus operations via disconnectors DS1, DS2, DS7, and DS9, and cross-interlocking states involving the 200 transfer bay. The empirical results confirm that all valid operational states execute correctly while invalid or unsafe switching commands are systematically blocked by the relay logic matrix.

As demonstrated in Table 2, the simulator perfectly executed all required functions without generating any false alarms or mechanical race conditions over repetitive cycles.

3.2. Protection function and quantitative parameter

The ability to meet stringent protection logic tests is the clearest evidence of the HIL architecture's performance:

(i) **50BF Function (Breaker Failure Protection):** To rigorously verify the 50BF logic, the testing framework integrates a numerical protection relay (specifically utilizing the ABB RET670 relay model deployed at the Bao Loc Substation) operating under a hybrid verification logic. The 50BF initiation scheme functions through a dual-criterion condition: the protection relay issues a start signal to its internal timers (t_1 and t_2) when a trip command is simultaneously combined with either persistent fault current ($I > I_{set}$) or an unasserted auxiliary contact (52a). During the breaker failure simulation test, the OMICRON CMC 356 injects a sustained fault current into the relay's analog input channels while the trip command destined for the simulator is deliberately isolated. This forces the intermediate relay's 52a contact to remain artificially asserted (closed), compelling the 50BF timers (t_1 set to 150 ms and t_2 set to 250 ms) to time out and successfully execute the backup tripping sequence to adjacent breakers. Across 30 repetitive test iterations, the inherent electromechanical latency was measured with high statistical repeatability at a mean of $\Delta t = 12.5$ ms with a standard deviation of ± 0.8 ms. This tightly bounded response time is significantly faster than the physical clearance window of actual high-voltage circuit breakers (40 - 60 ms), guaranteeing that 50BF initiation signals are safely reset before timer thresholds expire, thereby empirically proving complete immunity to race conditions.

(ii) **Trip Circuit Supervision Function (F74):** The 72-hour continuous test confirmed absolute current stability without drift, and intentional open-circuit testing validated the reliable drop-out response of the F74 supervision scheme. Thanks to the actual inductive characteristics of the intermediate relay coils, the supervision current is maintained continuously and realistically. This helps the F74 function operate extremely stably, eliminating false circuit break alarms [11].

(iii) **F79 Function:** Simulates the Close - Trip - Auto-Reclose cycle precisely according to the setting time without harming the actual circuit breaker [2].

3.3. Benchmarking and Quantitative Evaluation

To objectively illustrate the scientific novelty and technical advantages of the proposed intermediate-relay based simulator compared to current commissioning techniques, Table 3 presents a quantitative benchmarking comparison. The criteria are established based on actual commissioning requirements for a standard 220 kV bay.

As shown in Table 3, the scientific novelty of the proposed solution is quantitatively demonstrated through three main aspects. First, it provides a full-bay simultaneous I/O capacity (>30 I/Os) that standard commercial test sets cannot cover without expensive hardware extensions. Second, it maintains an optimized measured latency of 10-15 ms, which is intentionally faster than actual mechanical breakers (40-60 ms) to avoid 50BF timer race conditions, yet avoids the unrealistic <1 ms instantaneous response of purely digital solid-state simulators. Finally, it reduces the mechanical operations of the actual primary equipment during complex tests (such as 50BF and F79) to zero, thereby

eliminating mechanical wear while maintaining an extremely low fabrication cost (~\$500).

Table 3. Quantitative benchmarking of 220 kV bay testing methods

Evaluation Criteria	Traditional Method (Actual Equipment)	Commercial Test Sets (e.g., Omicron/ Doble)	Proposed Relay-Based Simulator
Supported Signal Type	Actual hardwired I/O	Low-level binary & Analog (CT/VT waveforms)	Hardwired binary I/O
Simultaneous I/O Capacity	Full bay	Limited (Typically 10-20 I/O ports)	Full bay (>30 I/Os for 1 CB, 4 DS, 2 ES)
Measured Latency	40-60 ms (Mechanical CB)	< 1 ms (Solid-state/Digital)	10-15 ms (Electromechanical)
Primary Equipment Operations (during 50BF/F79 tests)	> 10 times per scheme	0	0
Average Testing Time per Bay	3-5 days (Dependent on outage schedule)	1-2 days	1-2 days (Independent of primary eq.)
Estimated Hardware Cost	High (Associated with outage costs)	~\$20,000 - \$50,000+	~\$500 (Relays and wiring materials)

(Source: Author's compilation)

4. Economic- technical efficiency evaluation and application potential

4.1. Technical and operational efficiency

The practical application of the HIL simulator at Bao Loc 220 kV Substation has proven its superiority in resolving testing bottlenecks: *Firstly*, proactive commissioning scheduling. The system significantly reduces dependency on the construction progress of primary equipment in the switchyard. SCADA and relay engineers can independently configure databases, verify interlocking loops, and test HMI interfaces directly within the control room [2], [3]. *Secondly*, protection of the primary equipment lifecycle. According to CIGRE statistics, redundant mechanical operations during testing are a leading cause of premature aging in extra-high voltage circuit breaker drive systems [12]. By avoiding the need for actual circuit breaker switching during 50BF and F79 tests, the simulator removes risks of mechanical jamming and trip coil failure, thereby significantly extending the asset's operational lifespan and strictly complying with electrical safety regulations [2], [3]. *Thirdly*, a 'clean' testing environment. By providing physical I/O contacts with a defined latency of 10-15 ms, the simulator creates an isolated and reliable testing environment. If logic errors occur during testing, engineers can immediately isolate the cause within the secondary system (such as software configuration or panel wiring) without being interfered with by mechanical fault factors from external equipment.

4.2. Economic efficiency and expansion potential

Firstly, resource and cost optimization. Empirical data recorded during the Bao Loc 220 kV Substation upgrade project highlights significant efficiency gains. Traditionally, commissioning a 220 kV bay requires a 4-person engineering team working for 3-5 days, heavily

contingent on scheduled primary equipment outages. By utilizing the proposed simulator, the required testing duration was drastically reduced to just 1.5 days, executable by a 2-person team directly within the control room. Furthermore, the material cost for constructing the entire relay-based simulator is extremely economical (approximately \$500), making it overwhelmingly more cost-effective than deploying expensive multi-port commercial test sets or RTDS systems, while completely eliminating the unquantifiable costs associated with primary equipment outage time.

Secondly, scalability. The modular architecture of the simulator allows for effortless expansion of I/O capacity, enabling its application to more complex bay configurations at the 500 kV extra-high voltage level, such as the 3/2 breaker-and-a-half scheme.

Thirdly, educational application. Beyond its role in commissioning, this physical simulator serves as an invaluable visual educational tool. It provides a safe practice environment for junior engineers and operation personnel to familiarize themselves with SCADA interlocking operations and protection control system troubleshooting without posing any risks to the actual power grid.

4.3. System Limitations

While the proposed simulator offers significant advantages for logic and SCADA testing, its scope is strictly limited to hardwired binary I/O simulation. The system exhibits several inherent constraints:

Firstly, no analog simulation: The device does not generate continuous CT/VT waveforms or simulate transient faults. For full-scale protection testing requiring dynamic fault current/voltage injection, commercial secondary test sets remain irreplaceable.

Secondly, kinematic and mechanical constraints: The intermediate relays cannot replicate the exact mechanical kinematics of main contacts, such as contact bounce, pre-striking, or specific pole discrepancy characteristics (unless manually configured).

Thirdly, electromechanical delay constraints: Although the 10-15 ms latency is optimized for preventing 50BF timer race conditions, it is a fixed attribute of the selected relays and cannot be dynamically adjusted to simulate varying degrees of mechanical degradation of the primary circuit breaker.

5. Conclusion

This study has successfully designed, mathematically modeled, and empirically validated an intermediate-relay-based equipment state simulator for 220 kV substation commissioning. By synthesizing the hardwired interlocking logic based on Boolean algebra, the system completely eliminates the necessity for hazardous repetitive mechanical operations of primary switchgear during functional tests.

The quantitative benchmarking results substantiate the system's core advantages: providing a full-bay simultaneous I/O capacity with an inherent electromechanical latency of 10-15 ms. This physical latency boundary ensures complete

immunity to race conditions during time-critical schemes like Breaker Failure (50BF), while the relay coil's intrinsic impedance (54-65 k Ω) inherently prevents false Trip Circuit Supervision (F74) alarms. Field implementation at the Bao Loc 220 kV Substation verified that the proposed solution reduced testing time from 4 days to 1.5 days and drastically cut hardware simulation costs to approximately \$500, offering overwhelming economic efficiency compared to commercial injection test sets.

However, the application scope is strictly limited to hardwired binary I/O simulation; the system does not generate analog CT/VT waveforms for transient fault analysis, nor does it replicate the exact contact-bounce kinematics of actual high-voltage circuit breakers. Future developments aim to expand this relay-matrix architecture to accommodate complex bay configurations at the 500 kV extra-high-voltage level, while continuing to serve as an in-depth visual training aid for power system operation personnel.

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