OPTIMAL PLACEMENT OF DYNAMIC VOLTAGE RESTORER – SOLID STATE FAULT CURRENT LIMITER COMBINATION FOR GLOBAL VOLTAGE SAG MITIGATION IN DISTRIBUTION SYSTEM

Bach Quoc Khanh

Hanoi University of Science and Technology; khanh.bachquoc@gmail.com

Abstract - One of popular and effective solutions to voltage sag mitigation is the use of custom power devices (CPD) like dynamic voltage restorers (DVR). On the other hand, fault current limiter (FCL) also has impacts on voltage sags caused by faults. This paper introduces a new combination between DVR and solid-state fault current limiter (SSFCL) that can further improve global performance of voltage sags due to faults in distribution system. The location of DVR-SSFCL combination is optimally selected basing on minimizing a global index - $SARFI_X$. In optimizing DVR-SSFCL combination's placement, various cases of parameters relating with its ratings are considered and discussed. The paper uses IEEE's 33-bus distribution system for modeling voltage sag due to faults and DVR-SSFCL combination's effectiveness on global voltage sag mitigation.

Key words - distribution system; voltage sag; dynamic voltage restorer; solid-state fault current limiter.

1. Introduction

Voltage sag, according to IEEE1159 [1], is a phenomenon of power quality (PQ) in which the rms value of the voltage magnitude drops below 0.9 pu in less than 1 minute. Short-circuits in the power systems account for more than 90% of voltage sag events. Various solutions to voltage sag mitigation [2], [3] have been introduced, particularly for distribution system, and they are basically clustered into two groups [4] named "distributed improvement" and "central improvement" (or global improvement). While the first are mainly applied to protecting a single sensitive load, the later are introduced for globally (or totally) enhancing PQ in the distribution system (i.e. not only for a single load, but also for many loads). These solutions have recently attracted more and more interest from utilities as the cost of solutions has gradually declined.

With the recent development of power electronic applications, using the custom power device (CPD) for mitigating voltage sag is popular. Various researches on the CPD application with regard to the Dynamic Voltage Restorer (DVR) for either distributed improvement and central improvement of voltage sag have been introduced [5] - [12].

On the other hand, nowadays, the short circuit fault can generate fault current more than 20 times the maximum nominalcurrent that results in much higher thermal or mechanical stress for the affected equipment and the application of fault current limiter is emerging as one of the most effective solutions [13] - [14]. Knowing that for voltage sag due to short-circuits in power systems, any solution that changes the short-circuit current can also result in positive impacts on voltage sag situation and the application of fault current limiter is also a case. Regarding the FCL's effectiveness on voltage sag mitigation, there have been typical interesting researches [15] - [18]. [15] - [17] that considered dynamic modeling of FCL on voltage sag only. [18] proposed an optimal model for selecting FCL's location, but the consideration on voltage sag is only on the vulnerable area and voltage sag magnitudes.

This paper introduces a new method for global voltage sag mitigation by using a combination of solid-state fault current limiter (SSFCL) and DVR in distribution systems. It is an new expansion of [9] that considers additionally SSFCL's effectiveness on voltage sag mitigation in combination with DVR. This method optimizes the placement of the SSFCL-DVR combination basing on minimizing the global voltage sag index – $SARFI_X$ [19] caused by short-circuit events in the system of interest. The research uses the IEEE's 33-bus distribution feeder as the test system. Short-circuit calculation for the test system, the modeling of the SSFCL-DVR combinationfor global voltage sag mitigation as well as the modeling and solution to the problem of optimization are all programmed in Matlab.

Toward the above purpose, the paper is organised as follows: The Section 2 presents the proposal of the modeling of a SSFCL-DVR combination for short-circuit calculation and system voltage sag quantification in distribution system. The Section 3 defines the problem of optimization. Finally, the results for different scenarios of short-circuit events and the SSFCL-DVR combination's parameters are analysed in Section 4.

2. Modeling the SSFCL-DVR combination for short-circuit calculation

2.1. DVR modeling

DVR is a FACTS device that is connected in series with the load that needs to be protected or connected to the source generating PQ issues to limit its bad influence on the power system operation. The description of the DVR in the steady-state calculation is popularly given as a voltage source [3] connected in series with the impedance of the branch as Figure 1a. For steady-state calculation, a DVR is simulated as the model of the Norton's equivalent current source as Figure 1 b, c. [12].

Regarding DVR operation, Figure 2 presents three basic modes as follows [6]

- Protection mode: During fault, the DVR is protected from the high current in the load side due to short circuit on the load or large inrush currents, the DVR will be isolated from the system by using solid-state bypass switches (S2 and S3 will open) and providing an alternative path for current (S1 will be closed).

- Standby mode ($U_{DVR} = 0$): During normal operation, the DVR may either go into short circuit operation which is

called standby mode or inject small voltage to compensate the voltage drops on transformer reactance or losses.

- Injection/boost mode (U_{DVR}>0): As soon as sag is detected, the DVR goes into injection mode. AC voltage is injected in series with required magnitude, phase and wave shape for compensation.

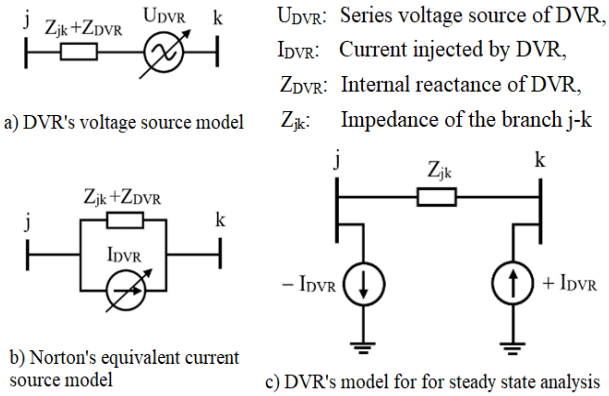

Figure 1. *DVR modeling*

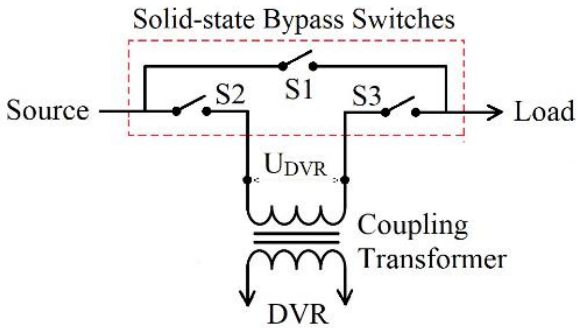

Figure 2. *DVR's operational modes*

2.2. Solid-state fault current limiter modeling

Application of FCLs is one viable approach to reduce thefault current. Under normal operating conditions, an FCL retains low impedance so that the power flow is unobstructed. In the event of a fault, however, the impedance of the FCLrapidly increases. Two types of FCLs are possible. An uninterruptingFCL reduces the fault current magnitude to an acceptable level, about 3-5 times the normal state maximum current, which, can be safely interrupted by the existing CB. An interrupting FCL can also act as a circuit breaker and interrupt the fault current. Uninterrupting-type FCLs are generally classified as passive, solid-state and hybrid types. With recent advances in high power semiconductor technology, various solid-state FLC (SSFCL) have been introduced. Three basic designs of SSFCL are series-switch, bridge and resonant types [13, 14].

No matter what type of SSFCL, the principle model of SSFCL can be used as Figure 3 [17] for analysis.

In short-circuits, the effectiveness of fault current limiting is made possible by presenting a large impedance in the system. The impedance is possibly either resistive or inductive components. Due to less demanding thermal management, inductive bypass is the preferred solution.

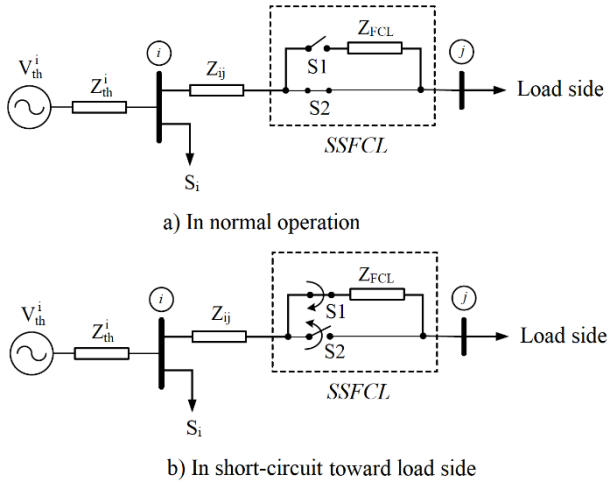

Figure 3. *SSFCL's operational modes*

2.3. Modeling of a combination of SSFCL and DVR

Basing on the modes of operation of DVR and SSFCL, their combination is introduced (Figure 4) where the bypass switch circuit S1 is placed with the FCL.

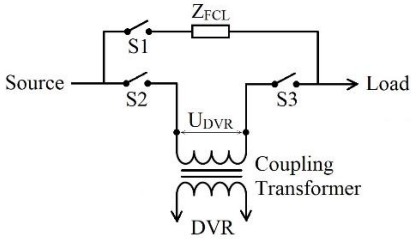

Figure 4. *DVR-SSFCL modeling*

For the protection mode of DVR where the DVR placed branch is a part of the short-circuit current carrying path, S1 is closed while S2 and S3 are opened, the SSFCL is introduced as the impedance Z_{FCL} for fault current limiting and it also impacts global voltage sag performance of the system. The standby mode and injection mode remain unchanged and DVR performs voltage sag mitigation as its desired applications.

2.4. Calculating short-circuit in power system with the presence of a SSFCL-DVR combination

Global voltage sag is assessed on short-circuit calculation in power systems and it is normally modeled using the method of bus impedance matrix [20]. Basing on the modeling of aSSFCL-DVR combination(FDC) as introduced in section 2.3, modeling the power system with the presence of a SSFCL-DVR combination for short-circuit calculation and voltage sag performance assessment is the integration of two integral parts.

- The first part corresponds to the performance of global voltage sag mitigation if the FDC is placed on the short-circuit current carrying path. For this part, DVR is disabled as switches S2 and S3 are opened while FCL is activated as switch S1 is closed. FDC acts as a SSFCL for limiting the fault current. In short-circuit calculation, the bus impedance matrix is modified with regard to adding the FCL's impedance. This paper considers FCL as a reactor.

- The second part corresponds to the performance of global voltage sag mitigation if the FDC is not placed on the short-circuit current carrying path. In this case, FCL is disabled by opening switch S1 while DVR is activated by closing switches S2 and S3. The DVR's effectiveness for global voltage sag mitigation is assessed by the application of the superposition principle according to the Thevenin theorem for the problem of short-circuit calculation in distribution system [20]. The bus voltage equation should be modified as follows [9]:

$$[U] = [Z_{bus}] \times ([I^0] + [\Delta I]) = [Z_{bus}] \times [I^0] + [Z_{bus}] \times [\Delta I] = [U^0] + [\Delta U] \quad (1)$$

where

$$[\Delta U] = [Z_{bus}] \times [\Delta I] \quad (2)$$

$$\text{or} \begin{bmatrix} \Delta\dot{U}_1 \\ \vdots \\ \Delta\dot{U}_k \\ \vdots \\ \Delta\dot{U}_n \end{bmatrix} = [Z_{bus}] \times \begin{bmatrix} \Delta\dot{I}_1 \\ \vdots \\ \Delta\dot{I}_k \\ \vdots \\ \Delta\dot{I}_n \end{bmatrix} \quad (3)$$

ΔU_i: Bus i voltage improvement (i=1÷n) after adding the custom power devices in the system.

ΔI_i: Additional injected current to the bus i (i=1÷n) after adding the custom power devices like DVR in the system.

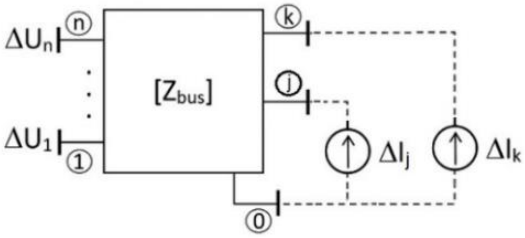

Figure 5. *Test system modeling using [Z_{bus}] with the presence of one DVR*

Assuming a DVR is placed on the branch j-k. Basing on the DVR modeling in Figure 5, in the matrix of additional injected bus current (3), there are only two elements that do not equal zero. They are $\Delta I_k = + I_{DVR}$ and $\Delta I_j = -I_{DVR}$. Other elements equal zero ($\Delta I_i = 0$ for i=1÷n, i≠j and i≠k).

Replacing the assumed values of ΔI_i in (3), we get

$$\Delta\dot{U}_k = Z_{kk} \times \Delta\dot{I}_k + Z_{kj} \times \Delta\dot{I}_j = (Z_{kk} - Z_{kj}) \times \dot{I}_{DVR} \quad (4)$$

According to the DVR modeling in Figure 1, the voltage of bus k is compensated up to the desired value. [9] proposes the desired value is 1pu. It means the bus k voltage is boosted by DVR from $U_k^0 = U_{sag.k}$ to U_k = 1p.u. So, $\Delta\dot{U}_k = 1 - \dot{U}_{sag.k}$ (5)

Replacing (5) into (4), we get I_{DVR}

$$\dot{I}_{DVR} = \Delta\dot{I}_k = \frac{\Delta\dot{U}_k}{Z_{kk} - Z_{kj}} = \frac{1 - \dot{U}_{sag.k}}{Z_{kk} - Z_{kj}} \quad (6)$$

- If I_{DVR} calculated by (6) is not greater than a given I_{DVRmax}, the voltage of bus k is boosted up to 1p.u. And the upgraded voltage for other bus i (i=1÷n; i≠k) in the test system can be calculated as follows

$$\Delta\dot{U}_i = Z_{ik} \times \Delta\dot{I}_k + Z_{ij} \times \Delta\dot{I}_j = (Z_{ik} - Z_{ij}) \times \dot{I}_{DVR} \quad (7)$$

- If I_{DVR} calculated by (6) is greater than I_{DVRmax}, the voltage of bus k is calculated as follows

$$\dot{U}_k = (Z_{kk} - Z_{kj}) \times \dot{I}_{DVRmax} + \dot{U}_{sag.k} < 1p.u. \quad (8)$$

The upgraded voltage for other bus i (i=1÷n; i≠k) in the test system can be calculated as follows

$$\Delta\dot{U}_i = (Z_{ik} - Z_{ij}) \times \dot{I}_{DVRmax} \quad (9)$$

Finally, bus voltages with the presence of DVR

$$\dot{U}_i = \Delta\dot{U}_i + \dot{U}_{sag.i} \quad (10)$$

3. Problem Definition

3.1. The test system

For simplifying the introduction of the new method in the paper, the IEEE 33-bus distribution feeder (Figure 6) is used as the test system because it just features a balanced three-phase distribution system, with three-phase loads and three-phase lines.

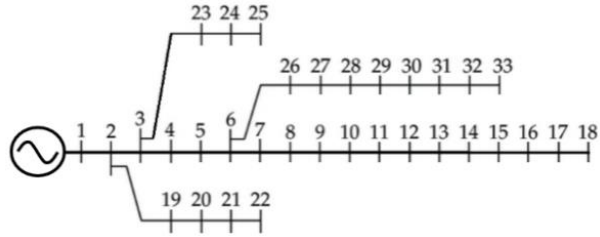

Figure 6. *IEEE 33-bus distribution feeder as the test system*

This research assumes base power to be 100MVA. Base voltage is 11kV. The system voltage is 1pu. System impedance is assumed to be 0.1pu.

3.2. Short-circuit calculation

The paper only considers voltage sags caused by fault. The effectiveness of global voltage sag mitigation is assessed on the system index - $SARFI_X$, that considers all possible fault positions in the test system. However, to simplify SARFIx calculation, we can consider only three-phase short-circuits. Other short-circuit types can be considered similarly if detailed calculation is needed.

Three-phase short-circuit calculations are performed in Matlab using the method of bus impedance matrix. The resulting bus voltage sags with and without the presence of FDC can be calculated for different scenarios of influential parameters as analysed in Part 4.

3.3. The problem of optimization

3.3.1. Objective function

In this research, the problem of optimizing the location of one FDC in the test system is introduced where the objective function is to minimize the System Average RMS Variation Frequency Index – $SARFI_X$ where X is a given rms voltage threshold [13].

$$SARFI_X = \frac{\sum_{i=1}^{N} n_{i.X}}{N} \Rightarrow \text{Min} \quad (11)$$

Where:

$n_{i.X}$: The number of voltage sags lower than X% of the load i in the test system.

N: The number of loads in the system.

For a given fault performance (fault rate distribution) of a given system and a given threshold X, $SARFI_X$ calculation is described as the block-diagram in Figure 7.

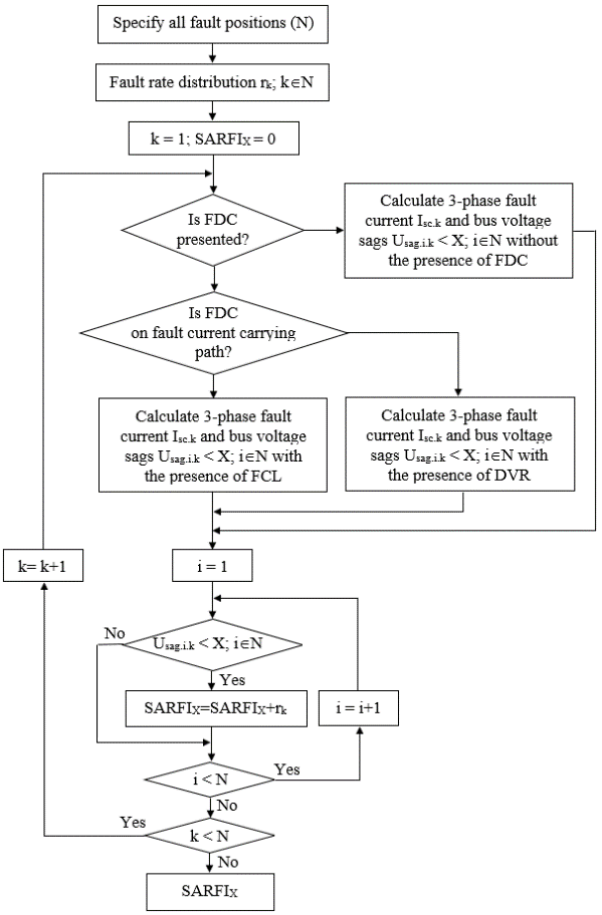

Figure 7. *$SARFI_X$ calculation*

For this problem of optimization, the main variable is the scenario of positions (branch) where FDCisplaced.

We can see each main variable as the branch numbers with FDCplacement out of the set of M branches of the test system. Therefore, the total scenarios of FDC placement to be considered is M=32 for the test system. For this problem, no constraint is set up.

3.3.2. Problem solving

For such a problem of optimization, with preset parameters (X%, SSFCL's impedance, DVR' limited current), the objective function – $SARFI_X$ is always determined. So, we use the method of direct search and testing all 32 scenarios of SSFCL positions. The block-diagram of solving this problem in Matlab is given in Fig.8.

For a candidate scenario k where the FDC is placed on the branch k, firstly, we check to see whether branch k is a part of the short-circuit current carrying path or not. Then we perform short-circuit calculation with the presence of FDC (as a FCL or a DVR) and nodal voltage sag that results in $SARFI_X$.

In the block-diagram, input data that can be seen as the above said preset parameters. "postop" is the intermediate variable that fixes the scenario of FDC position corresponding to the minimum $SARFI_X$. The initial solution of objective function Min equals B (e.g. B=33) which is big value for starting the search process. All calculations are programmed in Matlab. The scenarios for preset parameters are considered.

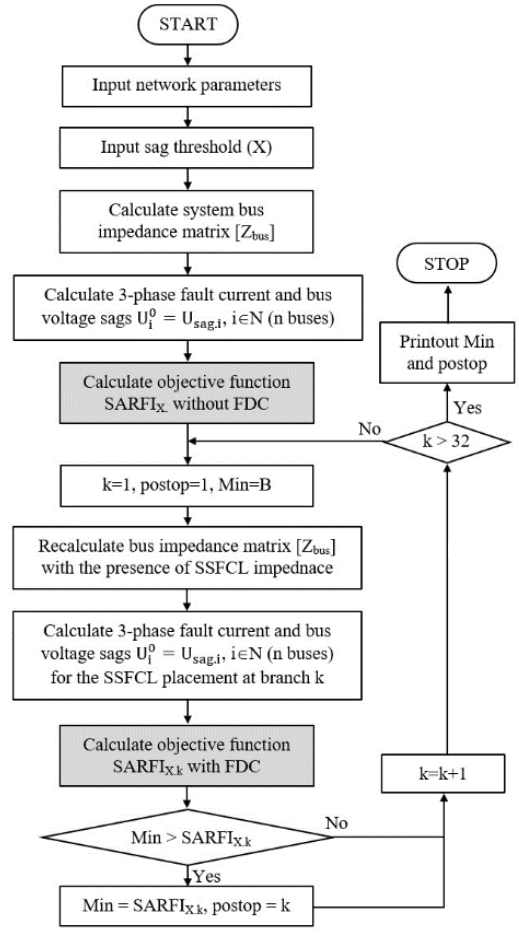

Figure 8. *Flowchart of the problem of optimization for selecting FDC's location*

4. Result Analysis

4.1. Preset parameters

The research considers the following parameters:

- For calculating $SARFI_X$, we need to know the fault rate distributed to all fault position. The paper uses uniform fault distribution as per [21] and fault rate = 1 time per unit period of time at fault position (each bus).

- For rms voltage threshold, the paper considers voltage sags so X is given as 90, 80, 70% of U_n as it is applicable for use of ITI curve [19].

- For SSFCL's impedance (Z_{FCL}), the paper considers the reactance that equals 1, 2, 4 and 6pu.

- For DVR's limited current (I_{DVRmax}), the paper considers the following value 0.1, 0.2, 0.5, 1pu.

4.2. Results analysis

Solving the problem of optimization considering above saidpreset parameters, step-by-step results are introduced.

For example, we consider placing a FDC (with ZFCL = j4pu, IDVR max = 1pu) on the branch 10 (between bus 9 and bus 10). If the fault location at bus 18, the FDC is on fault current carrying path (red marked in Figure 9) and FDC acts as FCL. The system bus voltage profile is plotted in Figure 10

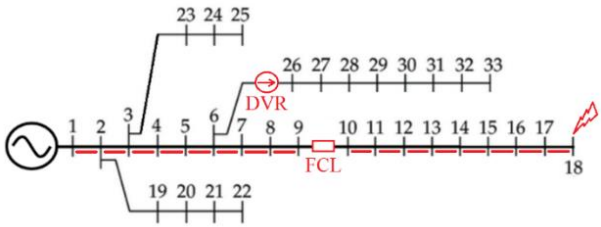

Figure 9. *Test system with fault current carrying path and optional locations of FDC*

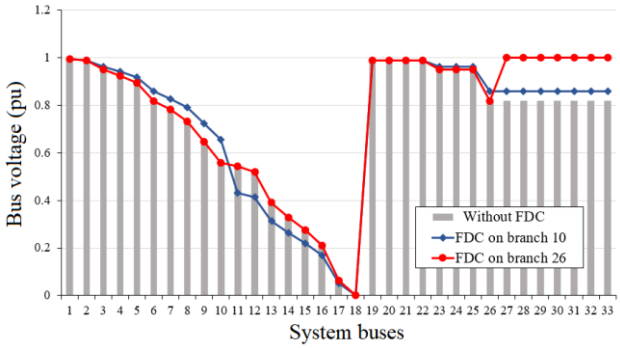

Figure 10. *System bus voltage profile for FDC on branch 10 and fault position at bus 18*

The introduction of FCL's impedance boosts the bus voltage from FCL's location to the source but it causes deeper voltage sag from its location to the fault position. If the FDC's location is on the branch 26 (between bus 6 and bus 26), FDC acts as a DVR and boost the voltage of bus 26 to 1pu, DVR's current is just 0.69pu< I_{DVRmax} =1pu. The system bus voltage profile is also plotted in Figure 10, the voltage is compensated upto 1pu for buses 26 to 33.

For a set of pre-set parameters and a scenario of FDC placement, $SARFI_X$ is calculated as Figure 7. Sag frequency for X=80%, Z_{FCL}=j4 puand I_{DVRmax}=1pu at all buses of the test system is depicted in Figure 11 for the cases: No FDC, DVR only and FDC on the branch 15. The $SARFI_{80}$ is 22.2424, 21.1515 and 20.8182 respectively.

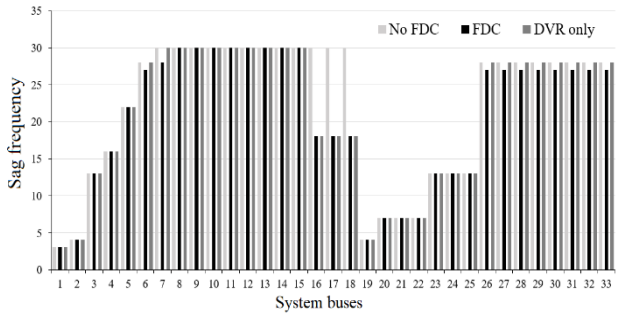

Figure 11. *Sag frequency without and with a FDC on the branch 15, X=80%, Z_{FCL}=j4pu and I_{DVRmax}=1pu*

Following the calculations as the flowchart in Figure 8, we can calculate $SARFI_X$ for all scenarios of FDC placement for different cases of pre-set parameters. Figure 12 is the $SARFI_{80}$ for different FCL's impedance while Figure 13 is $SARFI_{80}$ for different DVR's limited current for all scenarios of FDC placement. "0" means $SARFI_{80}$ without FDC.

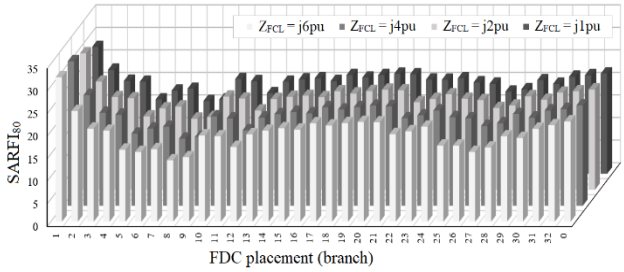

Figure 12. *$SARFI_X$, X=80%, I_{DVRmax}=1pu for different cases of FCL impedance (Z_{FCL})*

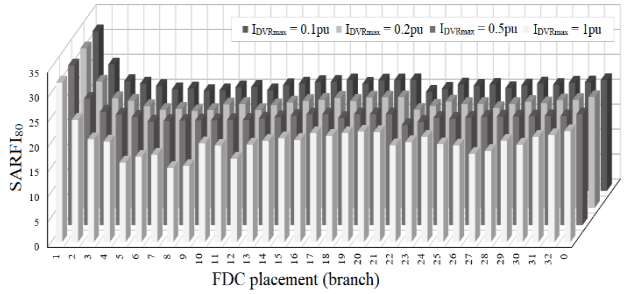

Figure 13. *$SARFI_X$, X=80%, Z_{FCL} = j4pu for different cases of DVR limited current (I_{DVRmax})*

Results are summarized in the following Table 1.

Table 1. *Result summary*

$SARFI_{70}$ = 18.5758	Z_{FCL} (pu)	1	2	4	6
	I_{DVRmax}=0.1pu				
	$SARFI_{X.min}$	17.1818	16.697	15.2727	15.2727
	Optimal place	27	27	25	25
	I_{DVRmax}=0.2pu				
	$SARFI_{X.min}$	16.7273	16.3333	14.9394	14.9091
	Optimal place	8	27	27	27
	I_{DVRmax}=0.5pu				
	$SARFI_{X.min}$	14.5758	14.5152	14.3333	14.2121
	Optimal place	12	12	12	12
	I_{DVRmax}=1pu				
	$SARFI_{X.min}$	13.0909	12.7576	11.7273	11.5758
	Optimal place	8	8	8	8
$SARFI_{80}$ = 22.2424	I_{DVRmax}=0.1pu				
	$SARFI_{X.min}$	21.1212	19.8788	19.8788	18.3333
	Optimal place	27	22	22	25
	I_{DVRmax}=0.2pu				
	$SARFI_{X.min}$	20.5758	19.697	19.4242	17.8485
	Optimal place	27	22	8	27
	I_{DVRmax}=0.5pu				
	$SARFI_{X.min}$	19.1515	18.7576	17.8485	16.2121
	Optimal place	6	6	6	6
	I_{DVRmax}=1pu				
	$SARFI_{X.min}$	16.1212	15.7576	14.8788	13.6364
	Optimal place	8	8	8	8

$SARFI_{90}$ = 24.8485				
	I_{DVRmax}=0.1pu			
	$SARFI_{X.min}$	24.1212	23.8788	21.9697	21.9697
	Optimal place	8	18	22	22
	I_{DVRmax}=0.2pu			
	$SARFI_{X.min}$	23.3939	23.1515	21.7879	21.7879
	Optimal place	27	27	22	22
	I_{DVRmax}=0.5pu			
	$SARFI_{X.min}$	21.3939	21.2121	21.0606	20.6667
	Optimal place	8	8	8	5
	I_{DVRmax}=1pu			
	$SARFI_{X.min}$	18.3636	18.1818	18.0303	17.9091
	Optimal place	8	8	8	8

Buses 6, 8, 25 and 27 are often selected as optimal locations for FDC placement as they are in the middle of the feeder. Finally, we can see that although DVR normally does not improve global voltage sag very much [9], with the presence of FCL, the global voltage sag is still much further improved.

5. Conclusion

This paper introduces a new method for further global voltage sag mitigation by using DVR in combination with SSFCL. DVR alone can improve global sag performance, but its effectiveness of global sag mitigation is somewhat limited as DVR can only compensate the voltage of buses from the DVR's location toward load side and it is also disabled if it is coupled on the fault current carrying path. With the presence of FLC, beside its main function of limiting the fault current, it can improve global voltage sag, and using the DVR protection mode circuit to introduce FCL can integrate the capability of global voltage sag mitigation from both devices. For mitigating by FCL function, the results show that FLC can cause deeper sags for buses from its location and fault position, but it improves voltage for buses between its location and the source and there is still room for improving global sag performance (reduction of $SARFI_X$). It depends on network configuration. The research can be further developed if FCL's main function (which is to reduce fault current) is included in the problem of optimization and a model of multi-objective optimization should be considered.

For the purpose of introducing the method, some assumptions are accompanied like the type of short-circuit and the fault rate distribution. For real application, the method can easily include the real fault rate distribution as well as all types of short-circuit.

REFERENCE

[1] IEEE Std. 1159-2009, IEEE Recommended Practice for Monitoring Power Quality (2009).

[2] A. Ghosh, G. Ledwich, Power quality enhancement using custom power devices, *Kluwer Academic Publishers*, London (2002).

[3] Math H. J. Bollen, Understanding power quality problems: voltage sags and interruptions, *IEEE Press*, John Wiley& Sons, Inc. (2000).

[4] M. Farhoodnea, et al., A Comprehensive Review of Optimization Techniques Applied for Placement and Sizing of Custom Power Devices in Distribution Networks, *Przegląd Elektrotechniczny* R. 88 NR. 11a, (2012).

[5] D. K. Tanti, M. K. Verma, B. Singh, O. N. Mehrotra, "Optimal Placement of Custom Power Devices in Power System Network to Mitigate Voltage Sag under Faults", International Journal of Power Electronics and Drive System, Vol.2, No.3, pp. 267-276, Jun. 2012.

[6] R. Pal, S. Gupta, "State Of The Art: Dynamic Voltage Restorer For Power Quality Improvement", Electrical & Computer Engineering: *An International Journal (ECIJ) Volume* 4, Number 2. Jun. 2015.

[7] R. Omar, N. A. Rahim, M. Sulaiman, "Dynamic Voltage Restorer Application for Power Quality Improvement in Electrical Distribution System: An Overview", *Australian Journal of Basic and Applied Sciences*, 5(12), pp 379-396, Dec. 2011.

[8] S. H. Chaudhary, G. gangil, "Mitigation of voltage sag/swell using Dynamic voltage restorer", IOSR Journal of Electrical and Electronics Engineering, Volume 8, Issue 4, pp 21-38, Nov-Dec. 2013.

[9] B. Q. Khanh, N. V. Minh, "Using the Norton's Equivalent Circuit of DVR in Optimizing the Location of DVR for Voltage Sag Mitigation in Distribution System", *GMSARN International Journal*, Vol.12, No. 3, pp 139-144, Jun 2018.

[10] M. A. Ali, M. Fozdar, K. R. Niazi, A. R. Phadke, "Optimal Placement of Static Compensators for Global Voltage Sag Mitigation and Power System Performance Improvement", *Research Journal of Applied Sciences, Engineering and Technology*, Vol.10, No.5, pp. 484–494, Jun. 2015.

[11] Y. Zhang, J. V. Milanovic, "Global Voltage Sag Mitigation With FACTS-Based Devices", *IEEE Transaction on Power Delivery*, Vol.25, No.4, pp. 2842–2850, Oct. 2010.

[12] T. Ratniyomchai, T. Kulworawanichpong, "Steady-State Power Flow Modeling for a Dynamic Voltage Restorer" *in proceedings of 5th WSEAS, ICAEE, Prague, Czech Rep.*, Mar. 12-14, 2006.

[13] A. Neumann, Application of Fault Current Limiters, BERR report, pp. 3-14, 2007. Available at: http://www.ensg.gov.uk/assets/dgcg00099rep.pdf

[14] A. Abramovitz, K. M. Smedley, Survey of Solid-State Fault Current Limiters, *IEEE Trans. on Power Electronics*, Vol. 27, No. 6, June 2012. pp. 2770-2782.

[15] C.S. Chang, P.C. Loh, Designs synthesis of resonant fault current limiter for voltage sag mitigation and current limitation, *Proc. IEEE Power Engineering Society Winter Meeting*. Conference, Singapore, 23-27 Jan. 2000.

[16] J.S. Kim, S.H. Lim, J.C. Kim, J.F. Moon, A Study on Bus Voltage Sag Considering the Impedance of SFCL and Fault Conditions in Power Distribution Systems, *IEEE Trans. on App. Supercond.*, Vol. 23, No. 3, June 2013.

[17] B. Boribun and T. Kulworawanichpong, Solid-state fault current limiter for voltage sag mitigation and its parameters design, Latest Trends on Circuits, Systems and Signals, WSEAS, http://www.wseas.us/e-library/conferences/2010/Corfu/CSS/CSS-16.pdf.

[18] N. Shurui, T. Lijun; Q. Dayong, Optimal allocation of superconducting fault current limiters considering voltage sags mitigation, *Proc. 2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Hong Kong, China, 7-10 Dec. 2014.

[19] 1564-2014 IEEE Guide for Voltage Sag Indices.

[20] J. J. Grainger, W. D. Stevenson, Power System Analysis, McGraw-Hill, Inc. 1994.

[21] B. Q. Khanh, D. J. Won, S. I. Moon, "Fault Distribution Modeling Using Stochastic Bivariate Models For Prediction of Voltage Sag in Distribution Systems", IEEE Transaction on Power Delivery, Vol.23, No.1, pp. 347-354, Jan. 2008.

(The Board of Editors received the paper on 03/10/2018, its review was completed on 11/6/2019)