A SIMPLIFIED NEUTRAL-POINT VOLTAGE BALANCING OF A THREE-LEVEL NPC INVERTER

PHƯƠNG PHÁP CÂN BẰNG ĐIỆN ÁP ĐIỂM TRUNG TÍNH ĐƠN GIẢN CHO BỘ NGHỊCH LƯU 3 MỨC CẤU TRÚC DIODE KẸP

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Abstract - This paper presents an enhanced space vector modulation strategy for three-level neutral-point-clamped inverters, aiming to balance the neutral point voltage. By strategically utilizing redundant vector pairs to adjust switching state dwell times, the proposed method minimizes neutral point voltage fluctuations due to the impact of medium and small vectors. A control variable modulates the dwell time of these redundant vectors within each switching cycle to achieve this balance, especially under high power factor and large modulation index conditions. MATLAB/Simulink simulations validate the strategy's effectiveness, demonstrating significant reductions in neutral point voltage deviation and harmonic distortion of the current while maintaining stable operation across diverse power factors and modulation indices.

Key words - Neutral-point-clamped inverter; space vector modulation; neutral-point voltage balancing; redundant vectors; impact of medium and small vectors.

Tóm tắt – Bài báo này trình bày phương pháp điều chế vectơ không gian cải tiến cho bộ nghịch lưu ba mức cấu trúc diode kẹp, nhằm mục đích cân bằng điện áp điểm trung tính. Bằng cách sử dụng các cặp vectơ trùng lặp để điều chỉnh thời gian đóng/cắt của trạng thái chuyển mạch, phương pháp đề xuất giảm thiểu giao động điện áp điểm trung tính do tác động của các vectơ trung bình và nhỏ. Một biến điều khiển được sử dụng để làm thay đổi thời gian đóng/cắt của các vectơ trùng lặp này trong mỗi chu kỳ chuyển mạch để đạt được sự cân bằng này, đặc biệt là trong điều kiện hệ số công suất cao và chỉ số điều chế lớn. Kết quả mô phỏng bằng phần mềm MATLAB/Simulink xác nhận hiệu quả của phương pháp đề xuất, chứng minh sự giảm đáng kể độ lệch điện áp điểm trung tính và độ méo hài của dòng điện trong khi vẫn duy trì hoạt động ổn định trên các hệ số công suất và chỉ số điều chế khác nhau.

Từ khóa – Bộ nghịch lưu cấu trúc diode kẹp; điều chế vectơ không gian; cân bằng điện áp điểm trung tính; vectơ trùng lặp; ảnh hưởng của vectơ trung bình và nhỏ.

1. Introduction

Multilevel inverters have garnered considerable attention in medium and high-voltage applications owing to their notable merits over conventional two-level inverters. These benefits contain enhanced voltage handling ability, decreased *dv/dt* stress, superior harmonic performance, and diminished voltage stress across switches [1-3]. Among the various multilevel inverter topologies, the three-level Neutral-Point-Clamped (3L-NPC) inverter stands out as one of the most practical and widely implemented configurations, particularly in industrial motor drives and renewable energy systems [4-6]. The 3L-NPC architecture enables lower output harmonic distortion and reduced voltage stress on power semiconductor devices, making it especially suitable for high-power and medium-voltage environments.

Despite its advantages, a significant limitation of the NPC topology is the uneven distribution of voltages across the DC-link capacitors. This inequality can lead to a deterioration in the quality of the output voltage by increasing total harmonic distortion (THD), shortening capacitor lifespan, and elevating the risk of device failure due to uneven voltage stress. Consequently, while the 3L-NPC inverter offers notable benefits in terms of performance and efficiency, ensuring effective capacitor voltage balancing remains a critical area of research to guarantee reliable and stable system operation.

Several control strategies have been proposed to address the neutral-point voltage imbalance in 3L-NPC inverters. One approach involves using a separate voltage source for each capacitor, typically implemented using a rectifier circuit [7]. Although this method can directly address the imbalance, it significantly increases the inverter's bulk and cost. In [8], the authors implemented an auxiliary power circuit to counterbalance the capacitor voltage on the DC-link. While effective in mitigating imbalance, this technique adds complexity, increases system costs, and may degrade performance due to the additional components. The most economically viable solution lies in modifying the modulation technique itself, bypassing the need for extra hardware. This can be accomplished by employing a carrier-based pulse width modulation technique that cleverly injects a zero-series voltage into the carrier signal [9]. While this method is notably efficient and effective in correcting voltage discrepancies, it does present the challenge of increased computational complexity, which may require more sophisticated processing capabilities.

In the last several years, numerous studies have explored

the challenge of neutral-point voltage imbalance associated with 3L-NPC inverters, which is often affected by the use of medium and small voltage vectors. Numerous notable strategies have been proposed to address this issue, including generating virtual vectors [10], adjusting modulation parameters with feedback signals [11], and applying Finite Control Set Model Predictive Control (FCS-MPC) [12-15]. Despite their advanced capabilities, virtual vector [10] methods face several significant challenges that hinder their overall performance. These techniques are often plagued by increased total harmonic distortion (THD), complex calculations for dwell time, and heightened switching losses, all of which contribute to reduced efficiency and shorten the lifespan of the devices involved. On the other hand, the FCS-MPC provides remarkably quick dynamic responses, yet it demands intensive computational resources and highly accurate system models. This reliance makes it particularly vulnerable to variations in system parameters and other practical uncertainties encountered in real-world applications. Another drawback of the FCS-MPC is the variable switching frequency, which can lead to increased switching losses, reduced efficiency, and challenges in filter design. In contrast, feedback-based methods [11] have emerged as a compelling alternative, demonstrating both effectiveness and simplicity. They offer a favorable balance between control performance, computational demands, and ease of implementation, making them attractive for various applications. However, it is important to note that existing research has predominantly characterized control variables in a generalized manner without providing concrete implementations. Additionally, these studies often overlook sensitivity analyses that could help identify the most suitable adjustment factors under different circumstances. Furthermore, the efficacy of these feedback-based methods when faced with varying system parameters remains inadequately explored, leaving a degree of uncertainty regarding their reliability and performance in dynamic operating conditions.

To address the challenges posed by capacitor voltage imbalance, this paper presents a novel solution that specifically targets the influence of both small and medium voltage vectors for 3L-NPC inverters. This phenomenon becomes particularly pressing when operating under high power factor conditions and elevated modulation indexes, both of which contribute to significant neutral-point voltage deviation and oscillations in capacitor voltage. The proposed technique incorporates a specifically designed control variable within the space vector modulation (SVM) algorithm, enabling a dynamic adjustment of the dwell time assigned to redundant vectors via the adjustment element P. This innovative approach determines the polarity of the difference between DC-link capacitor voltages and the phase currents of the inverter. By strategically selecting the most suitable redundant switching vectors based on this assessment, the proposed method effectively mitigates neutral-point voltage deviations. As a result, the output voltage and current waveforms exhibit a remarkable improvement, characterized by enhanced sinusoidal quality and a substantial reduction in THD. Even under varying system parameters, the performance remains consistently robust. Notably, a comparative analysis reveals that the THD of the load current is diminished dramatically from 2.31% in the conventional method [1] to a mere 0.22% in the proposed approach. Furthermore, while the conventional method experiences neutral-point voltage deviations of 55 V and 3 V, respectively, the proposed approach maintains remarkably balanced neutral-point voltage deviations. This stability persists even amidst the implications of medium voltage vector influences, underscoring the efficacy of the introduced solution.

2. Space vector modulation (SVM)

2.1. Topology of 3L-NPC inverters

The 3L-NPC inverter structure, illustrated in Figure 1, comprises four IGBT switches along with their corresponding clamping diodes for each branch [1], [9]. This design enables the inverter to produce three distinct output voltage levels: $+E$, 0, and -E. As a result, it can achieve lower voltage fluctuations and reduced harmonic distortion compared to traditional two-level inverter designs.

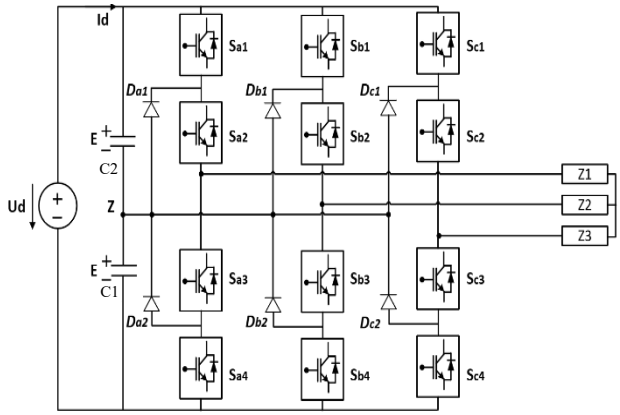


Figure 1. *Circuit structure of the 3L-NPC inverter*

In the NPC inverter, the DC-bus voltage is evenly divided between two capacitors, C_1 and C_2. The clamping diodes D_{a1} and D_{a2}, which are connected to the midpoint between the capacitors (Z), enable the generation of the neutral voltage level (0V). At any given moment, only two of the four switches in each inverter leg are conducting. To minimize switching losses, each switch is designed to transition only once per switching cycle, as described in [1]. The switching combinations of the three phases in a 3L-NPC inverter produce 27 distinct voltage vectors. These vectors are categorized into two types: those connected to the neutral point and those that are not. Vectors that interact with the neutral point affect the charging and discharging of the DC-link capacitors unevenly, resulting in a deviation in the neutral-point voltage (u_z). When this voltage deviates from zero, it can significantly impair the grade of the output voltage.

The first category includes the zero vectors, described by three conditions: PPP, OOO, and NNN. The second category consists of the small vectors, labeled $\vec{V}_1$ to $\vec{V}_6$. Each of these vectors has two redundant states: P-type (positive vector), such as POO, PPO, and OPO, and N-type (negative vector), like ONN, ONO, and NON. The third category includes the medium vectors, designated as $\vec{V}_7$ to $\vec{V}_{12}$, which are associated with states like PON, OPN, NPO, NOP, ONP, and PNO. Finally, the last category comprises

the large vectors, labeled $\vec{V}_{13}$ to $\vec{V}_{18}$, corresponding to states such as PNN, PPN, NPN, NPP, NNP, and PNP. Accurately classifying these vectors is crucial for the effective design of modulation strategies and for maintaining neutral-point voltage balance within the system.

2.2. Space vector diagram

Based on the identified voltage vectors, a space vector diagram with six sectors can be constructed, as shown in Figure 2. Each sector represents a 60-degree segment of the reference vector. Each sector involves the selection of an integration of large, medium, and small vectors to formulate the required reference vector.

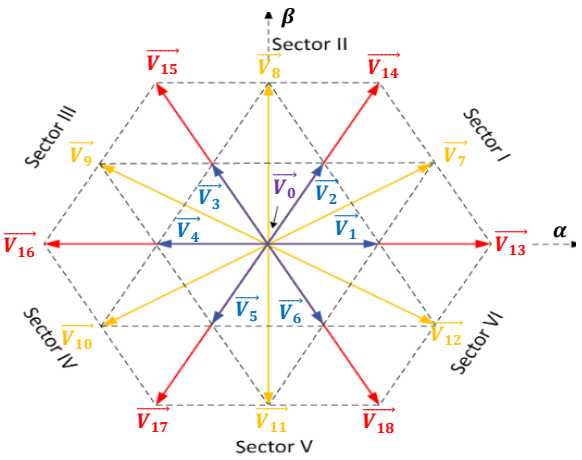


Figure 2. *Space vector diagram of the 3L-NPC inverter*

The selection of these vectors has a considerable influence on the variation of the neutral point voltage. Specifically, small and medium vectors are the main contributors to the oscillation of the neutral-point voltage during the implementation of space vector modulation. If P-type or N-type small vectors are not used symmetrically, this can cause a gradual shift of the neutral-point voltage in one direction, leading to an imbalance. Therefore, it is crucial to appropriately allocate the dwell times for these vectors within each switching cycle.

2.3. Effect on the neutral point voltage

When a P-type small vector (e.g., POO) is employed, the capacitor undergoes charging and discharging processes, which result in an elevation of the neutral point voltage. In contrast, using an N-type vector (e.g., ONN) causes charging and discharging that result in a decrease in the neutral point voltage. For medium vectors (e.g., PON), the impact on the neutral-point voltage depends on the load current and the specific switching state. Large vectors and zero vectors do not facilitate current flow through the neutral point and, consequently, exert no influence on the neutral-point voltage. Analysis shows that small and medium vectors directly affect the voltage at the neutral point. The next section will outline the proposed solution to address this issue.

3. Proposed compensation method

3.1. Control algorithm

Analyze the situation in Sector 1 - Region 2 of the space vector representation depicted in Figure 3. Within this area, the reference vector is constructed by integrating three proximate vectors: one medium vector (PON) and two small vectors (PPO - OON and POO - ONN).

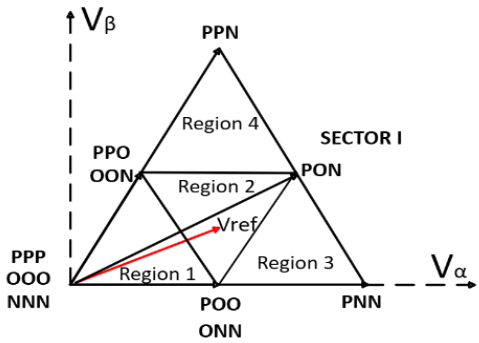


Figure 3. *Reference vector resides in region 2 within sector 1*

In this context, there are two pairs of redundant switching vectors [16]. These vectors produce identical output voltages but differ in the paths taken by the current flowing through capacitors C_1 and C_2, resulting in different effects on the neutral point voltage. For example, the vectors POO and ONN form one such redundant pair. The vector ONN generates a neutral current of $i_z = i_a$, while POO results in $i_z = i_b + i_c = -i_a$. Consequently, when $i_a > 0$, the POO vector causes an increase in the neutral point voltage, while the ONN vector causes it to decrease.

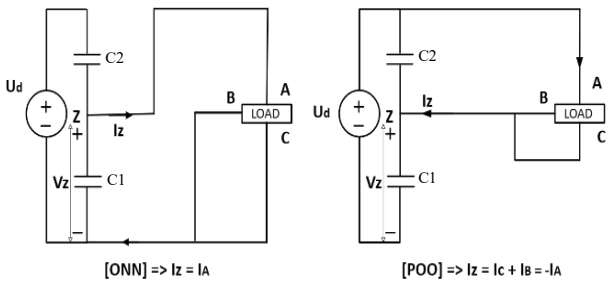


Figure 4. *Circuit diagrams corresponding to small vector types*

Table 1. *Classify redundant small switching vectors*

Vector	Positive (P-type)	i_z	Negative (N-type)	i_z
1	ONN	i_a	POO	-i_a
2	PPO	i_c	OON	-i_c
3	NON	i_b	OPO	-i_b
4	OPP	i_a	NOO	-i_a
5	NNO	i_c	OOP	-i_c
6	POP	i_b	ONO	-i_b

By observing the voltage difference between capacitors C_1 and C_2, along with the polarity of the phase currents i_a, i_b, and i_c, we can determine whether a specific redundant vector will increase or decrease the neutral-point voltage when applied. Positive vectors are defined as cases where the neutral current i_z equals the current of a specific phase, corresponding to the condition that only one phase is directly connected to the neutral point. Conversely, negative vectors are defined as cases where the neutral current i_z has the same magnitude but opposite direction to the current of a specific phase, corresponding to the condition that two phases are simultaneously connected to the neutral point. As a result, positive vectors cause an

increase in the neutral-point voltage (u_z), while negative vectors lead to a decrease in u_z. The classification of redundant vector pairs, as presented in Table 1, aids in determining the proper adjustment, either increasing or decreasing the dwell time, based on the algorithm illustrated in Figure 5 [11].

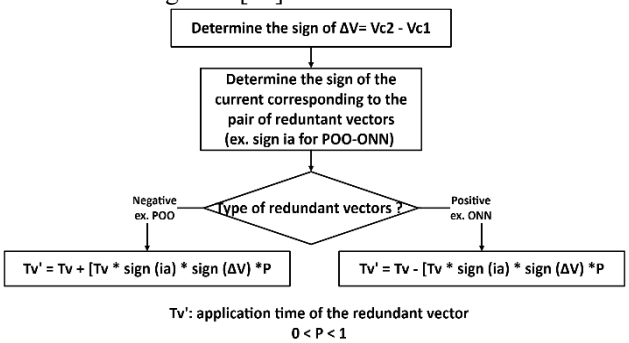


Figure 5. *Algorithm for determining the dwell time of redundant vectors*

3.2. Calculation of specific dwell time

After identifying the appropriate direction to adjust the dwell time for each redundant vector, the calculated times are directly applied to the switching sequence. Figure 6 provides an example of this allocation for region 2 in sector 1. In each sampling interval T_s the dwell times T_a, T_b, and T_c, which correspond to the voltage vectors $\vec{V}_1$, $\vec{V}_7$ and $\vec{V}_2$ respectively, are utilized to construct the desired reference voltage vector based on the following expression:

$$\begin{cases} T_s * \vec{V}_{\text{ref}} = T_a * \vec{V}_1 + T_b * \vec{V}_7 + \mathrm{T}_c * \vec{V}_2 \\ T_s = T_a + T_b + \mathrm{T}_c \end{cases} \quad (1)$$

With: $$\lambda_1 = \frac{T_a}{4} * sign(i_a) * sign(\Delta V) * P \quad (2)$$

$$\lambda_2 = \frac{T_c}{4} * sign(i_c) * sign(\Delta V) * P \quad (3)$$

Within a switching cycle, the arrangement of states and the distribution of their dwell times are critical for system performance. These intervals may be further subdivided, leading to specific terminologies such as $T_a/4$ and $T_c/4$ in the context of a symmetrical switching sequence. This sophisticated segmentation allows for finer control over the timing and transitions between states. When calculating the adjustment times λ_1 and λ_2, it is essential to maintain the ratio established by these subdivisions. However, to enhance the adaptability of the switching process, an additional coefficient, referred to as the adjustment factor P, is introduced. This factor explicitly represents the proportion of adjustment time with the original dwell time allocated to the redundant vectors. The introduction of P allows for seamless adjustments in the timings of λ_1 and λ_2 by simply altering the value of P. To maintain system stability and operational integrity, the variable P must adhere to the strict constraint $0 < P < 1$. This ensures that both λ_1 and λ_2 remain less than the original dwell time, thereby preventing any adjustments from surpassing permissible limits. Such careful regulation of P not only guarantees efficient adjustments but also sustains the overall reliability and safety of the switching process. In the other sectors, the values of λ_1 and λ_2 are determined using the dwell times and phase currents associated with their respective redundant vector pairs.

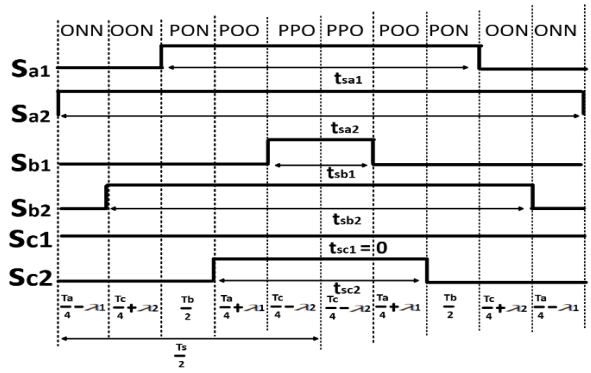


Figure 6. *The switching sequence and relevant dwell times for each state in region 2 of sector 1*

In order to reduce the total number of switching events, thereby prolonging the lifetime of the power switches and simultaneously minimizing switching losses, it is essential to arrange the switching states such that consecutive vectors differ by only a single switching action. This strategy ensures smoother transitions between states while avoiding unnecessary commutations. As a result, the switching states are systematically organized into a symmetrical sequence, where the dwell times are distributed in proportion to the reference vector position. This symmetrical arrangement not only balances the switching activity among the inverter legs but also contributes to reducing harmonic distortion in the output waveforms. Based on the dwell-time distribution of the symmetrical sequence (illustrated in Figure 6 for Region 2, Sector I), the switching durations corresponding to each inverter leg a, b, and c within one complete cycle can be explicitly determined as follows:

$$\begin{cases} \boldsymbol{t_{sa1}} = 2\left(\frac{T_b}{2} + \frac{T_a}{4} + \lambda_1 + \frac{T_c}{4} - \lambda_2\right) \\ \quad = \frac{T_a+T_c}{2} + T_b + 2(\lambda_1 - \lambda_2) \\ \boldsymbol{t_{sa2}} = 2\frac{T_s}{2} = T_s \\ \boldsymbol{t_{sb1}} = 2\left(\frac{T_c}{4} - \lambda_2\right) = \frac{T_c}{2} - 2\lambda_2 \\ \boldsymbol{t_{sb2}} = 2(\frac{T_c}{4} + \lambda_2 + \frac{T_b}{2} + \frac{T_a}{4} + \lambda_1 + \frac{T_c}{4} - \lambda_2) \\ \quad = T_s - \frac{T_a}{2} + 2\lambda_1 \\ \boldsymbol{t_{sc1}} = 0 \\ \boldsymbol{t_{sc2}} = 2\left(\frac{T_a}{4} + \lambda_1 + \frac{T_c}{4} - \lambda_2\right) \\ \quad = \frac{T_a}{2} + \frac{T_c}{2} + 2(\lambda_1 - \lambda_2) \end{cases} \quad (4)$$

Furthermore, the variable λ is constrained by the adjustment factor (P) [11]. A sensitivity analysis was conducted to obtain the results shown in Figure 7. Based on this analysis, the optimal adjustment factor was determined as $P = 0.7$, considering both the total harmonic distortion (THD) of the load current and the deviation of the neutral-point voltage (ΔU). The findings can be summarized as follows:

- Small values of P (0.1-0.5): THD of the load current is very low, but ΔU becomes excessively high, which is undesirable.

- Large values of P (0.8-1.0): ΔU is very low, but THD increases significantly, which is also not optimal.

- At $P = 0.7$: both THD and ΔU remain at moderately low levels, providing a favorable trade-off (THD=1.34%, $\Delta U = 0.9$).

Moreover, a sensitivity analysis was carried out by varying the load parameters ($cos\varphi$) and the modulation index (m_a). The results demonstrate that at $P = 0.7$, both the neutral-point voltage fluctuation and the load current THD vary only marginally (about 2%), confirming that the system maintains stable operation with high performance quality. The detailed results of this analysis are presented in Figures 11 and 12.

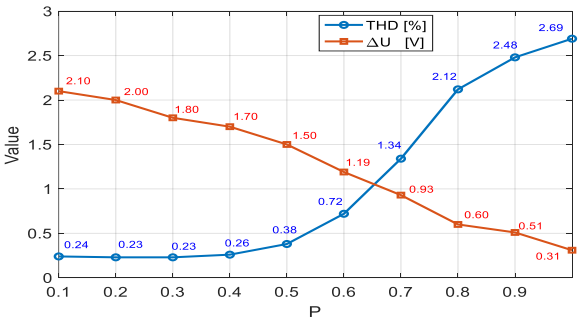


Figure 7. *Effect of the adjustment factor P on system performance for* $m_a = 0.8$ *and* $cos\varphi = 0.85$

4. Simulation verification

4.1. Constant modulation index and power factor

To validate the proposed neutral-point voltage balancing control method, a simulation was conducted using Matlab Simulink. A 3L-NPC inverter was constructed to supply a three-phase resistive load through an L-filter, utilizing the SimPowerSystems toolbox. The main parameters used in the simulation are provided in Table 2. The switching frequency for the 3L-NPC inverters is set at 10 kHz. The overall control strategy is illustrated in Figure 8.

Table 2. *Simulation parameters*

DC-voltage	500 V
Capacitance	3300 μF
Load	10 Ω, 20 mH
Switching frequency	10 kHz
Fundamental frequency	50 Hz
Adjustment factor	0.7
Modulation index	0.8
Power factor	0.85

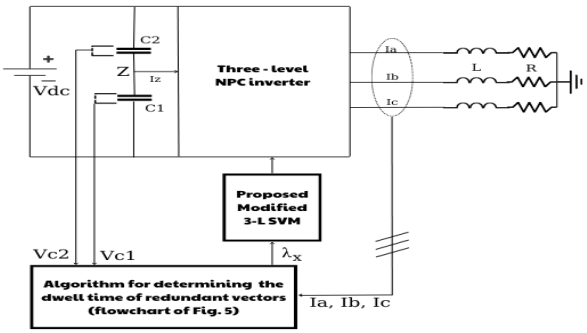
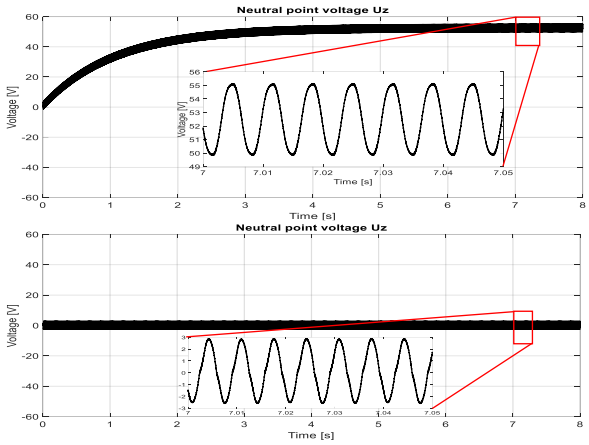
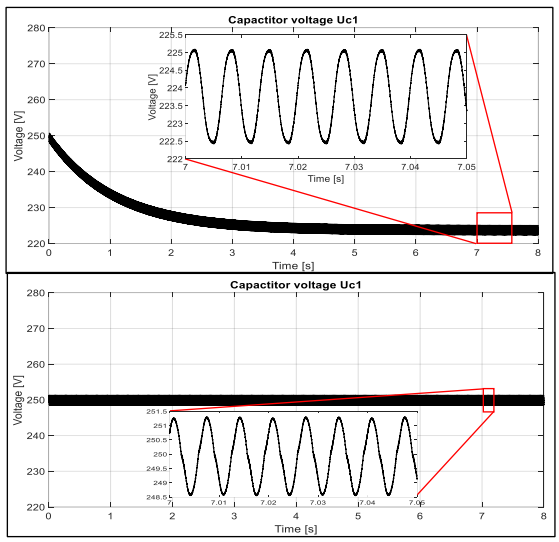


Figure 8. *Control diagram used for experimental validation*

Figure 9 presents a comprehensive analysis of the major advantages of the suggested approach, specifically the neutral-point voltage u_z and the upper capacitor voltage V_{c1}. This analysis compares the values obtained before and after utilizing the proposed dwell time adjustment algorithm. In Figure 9a, it is evident that before the adjustment, the neutral point voltage exhibited significant fluctuations, indicating instability within the system. Additionally, Figure 9b provides a closer look at the capacitor voltage difference, which also demonstrates a substantial improvement in post-adjustment. The voltage across the capacitors reaches a stable state, enhancing the overall efficiency and reliability of the system.



a)



b)

Figure 9. *a) Neutral point voltage before and after adjustment, b) Capacitor voltage* V_{c1} *before and after adjustment*

Figure 10 illustrates an assessment of the output responses before and after applying the proposed modulation technique. As observed in Figures 10a and 10c, the output voltage and load current exhibit notably reduced waveform distortion following the adjustment, resulting in smoother and more sinusoidal waveforms. This enhancement is attributed to improved neutral-point voltage balancing of the DC-link. Additionally, Figures 10b and 10d display the harmonic spectra of the voltage and current, indicating a noticeable reduction in THD. The comparative analysis indicates a pronounced improvement in harmonic performance, with the THD of the load current reduced from 2.31% using the conventional approach [1] to 0.22% under the proposed scheme. Moreover, while the conventional technique exhibits neutral-point voltage deviations of 55 V and 3 V, the proposed strategy effectively sustains a well-balanced neutral-point potential, even in the

presence of medium voltage vector influences, thereby substantiating the superior stability and efficacy of the developed control strategy. The noticeable decrease in THD for both voltage and current confirms that the implemented algorithm effectively mitigates unwanted harmonics, thereby improving the power quality of the system.

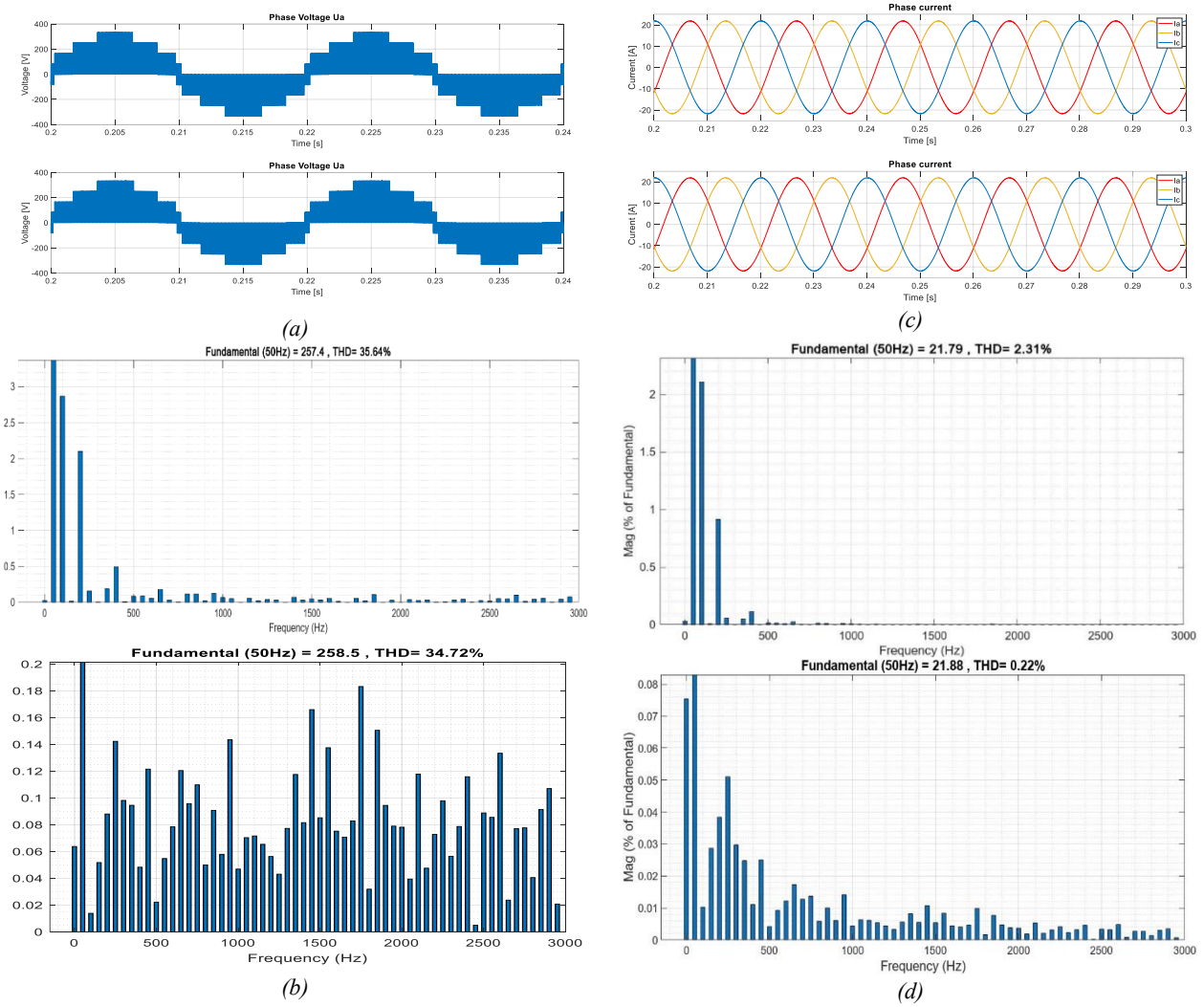


Figure 10. *Output response of the inverter before and after applying the proposed modulation technique. a) phase A voltage v_a, b) THD of phase A voltage v_a, c) phase current, d) THD of phase current*

Compared with the simulation results reported in [11] at a modulation index of m_a=0.8, the proposed method demonstrates a substantial enhancement in current quality, owing to the rigorous analysis and optimal adjustment of the factor introduced in Section 3.2. The output current waveform approaches an almost ideal sinusoid with only negligible distortion, representing a notable advancement over conventional approaches. This performance gain is particularly impactful for grid-connected scenarios where stringent current quality is essential, such as renewable energy conversion systems (solar PV and wind power) and high-performance motor drive applications, thereby underscoring the practical relevance and robustness of the proposed strategy.

4.2. Modulation index and power factor variations

This section will examine some cases involving variations in the modulation index and power factor to assess their impact on voltage and current quality after applying the proposed method.

Figure 11 illustrates the relationship between the power factor cosφ and its effects on THD of the phase current i_a, as well as the ripple amplitude of the neutral-point voltage u_Z. The findings indicate that as the power factor cosφ decreases, specifically falling below optimal levels, the THD of i_a, also shows a corresponding decrease. This suggests improved current quality with lower distortions. Conversely, the neutral-point voltage deviation increases slightly; however, it remains at a low level [17], particularly in the narrow range of power factor values between 0.8 and 0.9. Figure 12 illustrates the effect of the modulation index m_a on system quality at a power factor of cosφ=0.85. The system exhibits optimal performance, characterized by low current THD and minimal DC-link voltage deviation when m_a is within the range of 0.85 to 0.9. However, when m_a exceeds 0.95, the ripple amplitude increases markedly. According to the proposed method, the maximum value of the neutral-point voltage deviation and the THD of the load current are 7.2V and 1.4%, respectively, under variations of parameters such as cosφ and m_a. These results demonstrate the effectiveness of the

proposed approach in meeting the limits of voltage deviation (3% Vdc) and THD (5%) for practical applications.

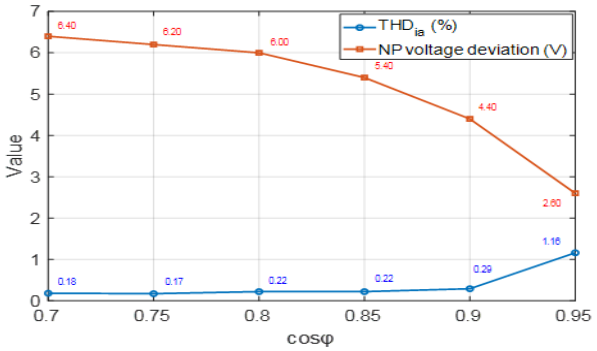


Figure 11. *Impact of cosφ on system quality*

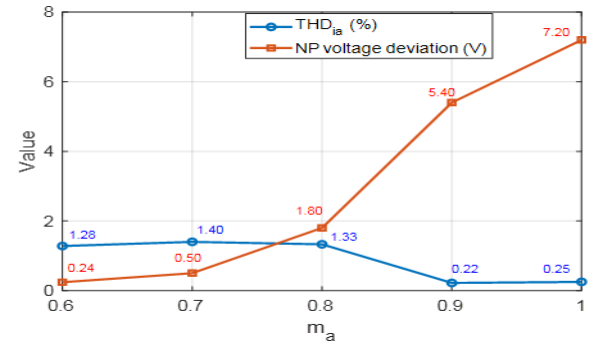


Figure 12. *Impact of modulation index ma on system quality*

Based on the data presented in the figures, this indicates that the proposed control method effectively maintains stable operation across a broad spectrum of m_a and power factor cosφ values. This stability is essential for ensuring high-quality voltage and current, even under a wide range of load conditions, especially with high modulation index and power factors. The control method's capability to adapt to varying operational parameters highlights its robustness and reliability, making it an excellent solution for applications requiring consistent electrical performance.

5. Conclusion

This paper proposes an enhanced SVM strategy for 3L-NPC inverters, whose primary contribution lies in achieving superior neutral-point voltage balancing through the optimized deployment of redundant vectors. The method strategically selects redundant switching vectors and adjusts their dwell times via the adjustment factor P, thereby mitigating neutral-point voltage fluctuations induced by medium and small vectors. Furthermore, a control variable λ is introduced to modulate the dwell time of redundant vectors within each switching cycle, ensuring effective voltage balancing, particularly under high power factor and large modulation index conditions. The simulation results demonstrate that the proposed method delivers significant enhancements in output voltage quality, current waveforms, and neutral-point voltage balancing. In particular, the THD of the load current is reduced from 2.31% with the conventional method to only 0.22% under the proposed scheme. Moreover, the neutral-point voltage deviations are substantially suppressed, decreasing from 55 V in the conventional approach to just 3 V with the offered strategy, thereby highlighting its superior effectiveness and robustness. The proposed approach is readily extendable to other multilevel inverter topologies, enabling broad applicability in renewable energy conversion systems and industrial motor drive applications. Future research will concentrate on experimental validation of the method and its integration with advanced control strategies to further enhance performance in practical industrial environments.

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REFERENCES

[1] B. Wu and M. Narimani, *High-power converters and AC drives*, 2nd edition. John Wiley & Sons, 2017.

[2] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, 2002.

[3] A. Poorfakhraei, M. Narimani, and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 155-170, 2021.

[4] H. Abu-Rub, A. Iqbal and J. Guzinski, *High performance control of AC drives with Matlab/Simulink*. John Wiley & Sons, 2021.

[5] F. Guo, T. Yang, C. Li, S. Bozhko, and P. Wheeler, "Active Modulation Strategy for Capacitor Voltage Balancing of Three-Level Neutral-Point-Clamped Converters in High-Speed Drives," *in IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2276-2287, 2022.

[6] M. Mollahasanoglu, H. Mollahasanoglu, and H. I. Okumus, "A New PWM Technique for Three-Phase Three-Level Neutral Point Clamped Rectifier," *Arabian Journal for Science and Engineering*, vol. 49, pp. 6521-6530, 2024.

[7] K. S. Kumar, K. Sukumar, K. Gopakumar, G. Mondal, and K. Corzine, "Neutral-point balancing of neutral-point-clamped three-level inverter with a front end switched rectifier DC source for the full modulation range," *IET Power Electronics*, vol. 2, no. 5, pp. 527-534, 2009.

[8] A. Shukla, A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for DC capacitor voltage balancing in diode clamped multilevel inverter," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2249-2261, 2010.

[9] B. Zhang, Q. Ge, L. Tan, X. Wang, Y. Yu, and J. Liu, " A New PWM scheme for loss balancing and neutral-point voltage balancing in three-level active NPC converter," *IEEE 10th Conference on Industrial Electronics and Applications (ICIEA)*, 2015, pp. 1128-1133.

[10] Q. Yuan, A. Li, J. Qian, and K. Xia, "DC-link capacitor voltage control for the NPC three-level inverter with a newly MPC-based virtual vector modulation," *IET Power Electronics*, vol. 13, no. 5, pp. 1093-1102, 2020.

[11] A. Zorig, S. Barkat, and A. Sangwongwanich, "Neutral Point Voltage Balancing Control Based on Adjusting Application Times of Redundant Vectors for Three-level NPC inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 5604-5613, 2022.

[12] C. Smith, A. Gargoom, M.T. Arif, and M.E. Haque, "Model predictive control of 3L-NPC inverter to enhance fault ride through capability under unbalanced grid conditions," *IET Power Electronics*, vol. 17, pp. 1973-1985, 2024.

[13] E. S. Jun, M. H. Nguyen, and S. S. Kwak, "Model Predictive Control Method with NP Voltage Balance by Offset Voltage Injection for Three-Phase Three-Level NPC Inverter," *IEEE Access*, vol. 8, pp. 172175–172195, 2020.

[14] S. Peng, G. Zhang, Z. Zhou, X. Gu, and C. Xia, "MPTC of NP-clamped three-level inverter-fed permanent-magnet synchronous motor system for NP potential imbalance suppression," *IET Electric Power Applications*, vol. 14, no. 4, pp. 658-667, 2020.

[15] I. M. Alsofyani and K. B. Lee, "Three level inverter fed model predictive torque control of a permanent magnet synchronous motor with discrete space vector modulation and simplified neutral point voltage balancing," *Journal of Power Electronics*, vol. 20, pp. 22-30, 2022.

[16] X. Yuan, Y. Gao, and Y. LI, "A Fast Multilevel SVPWM Method Based on the Imaginary Coordinate with Direct Control of Redundant Vectors or Zero Sequence Components," *IEEE Open Journal of the Industrial Electronics Society,* vol. 1, pp. 355-366, 2020.

[17] *Standard for Harmonic Control in Electric Power Systems*, IEEE 592-2022, 2022.